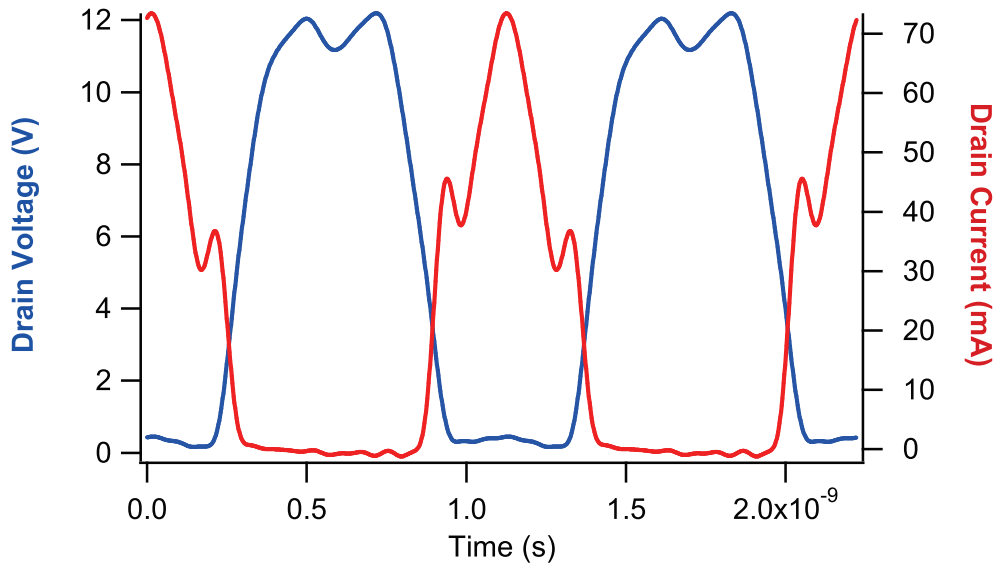
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Introduction to Waveform Engineering



Tudor Williams

Mesuro Limited, Pencoed Technology Park, Pencoed, CF35 5HZ UK

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Summary

- **Introduction to WaveForm Engineering**
- **Why do Waveform Engineering?**
- **How to Perform Waveform Engineering**
  - **Basics of Waveform Measurement**
  - **Basics of Waveform De-embedding**
  - **Basics of Waveform Shaping**
    - **Impedance Control – Load-pull and related architectures**
- **Waveform Engineering Case Studies**
- **Conclusions**

- **Designing Using Waveforms – Tutorial Class F Amplifier Design**

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Introduction to Waveform Engineering

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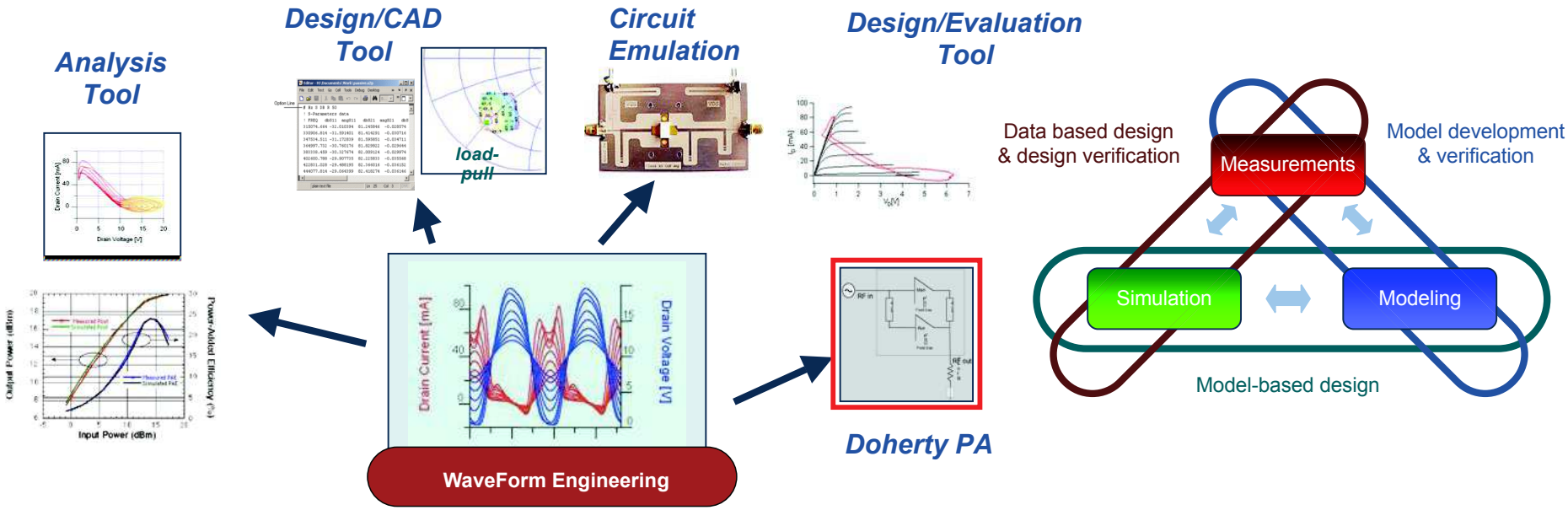
Introduction

- **WaveForm Engineering – A characterisation technique aimed at high power, non-linear devices, such as those used in communications/military systems.**
  - Feedback to manufacturers on new process development and improvement.
  - Direct application in design cycle of high efficiency, Power amplifiers.

- **Allows for a more scientifically driven approach to characterisation of high power non-linear devices.**
  - Reduce Time to Market
  - Reduce Engineering Resource
  - Improve efficiency and related costs!

WaveForm Engineering – Why?

‘ WaveForm Engineering – The ability to measure and shape the voltage and current waveforms of a test device or circuit.’

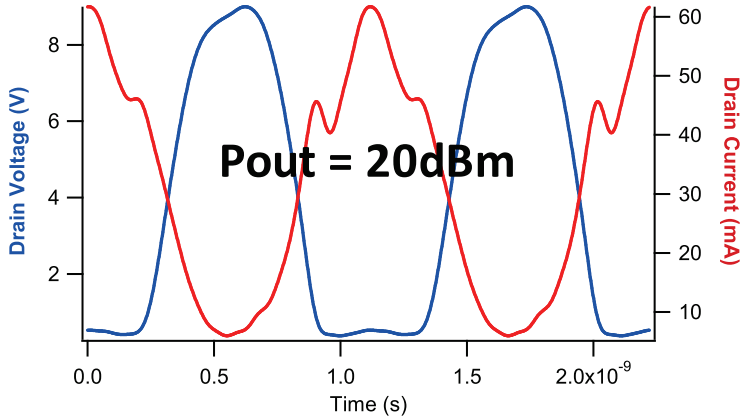


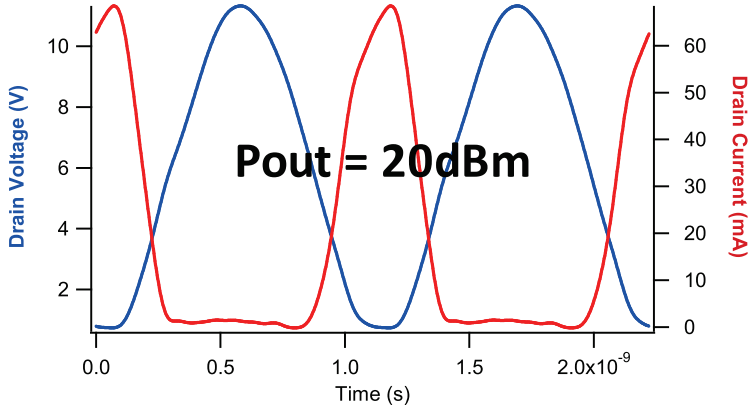
unifying link between device technology, circuit design & system performance

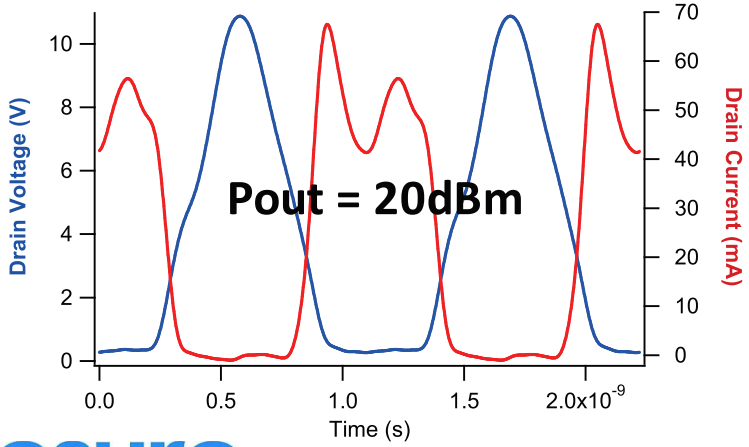
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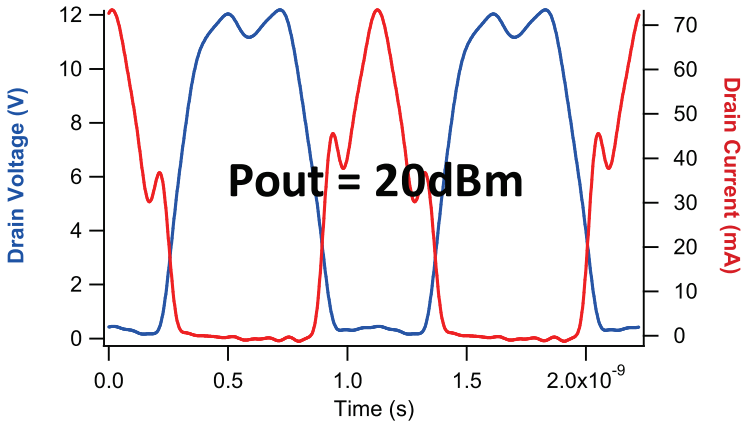
WaveForm Engineering – Why?

- **An output signal from a device at a single power level can be represented by an infinite set of current and voltage waveforms.**



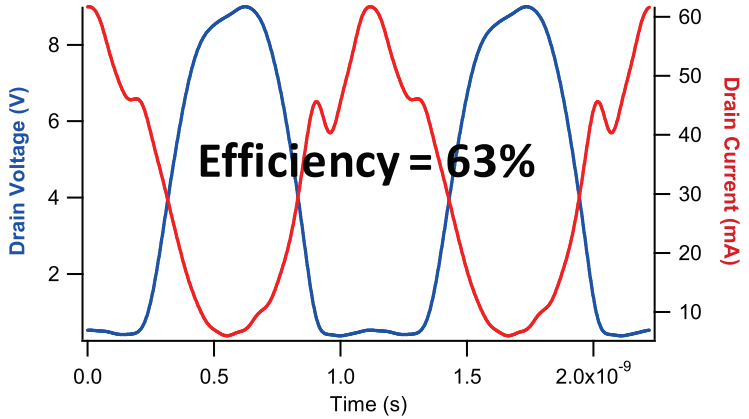


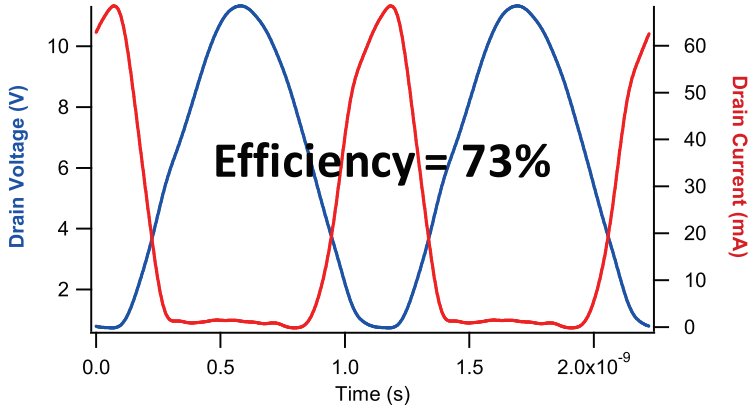


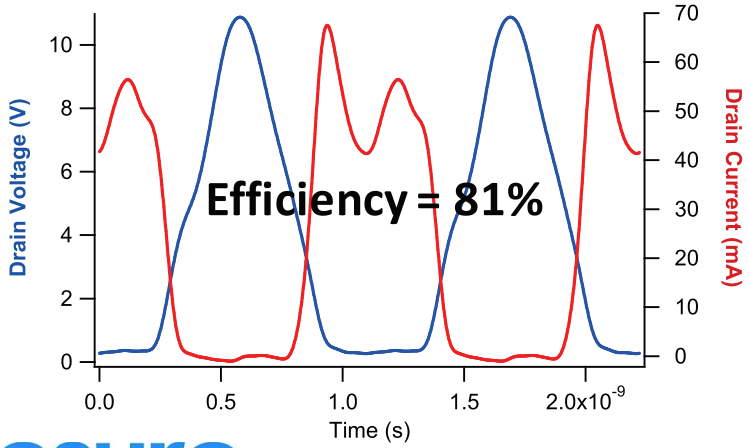


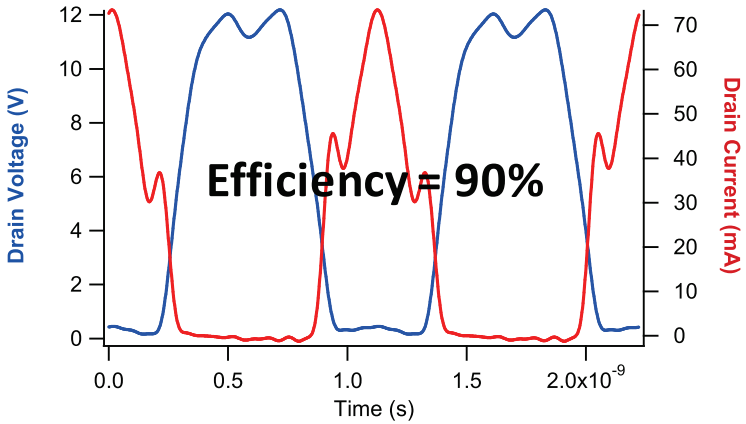
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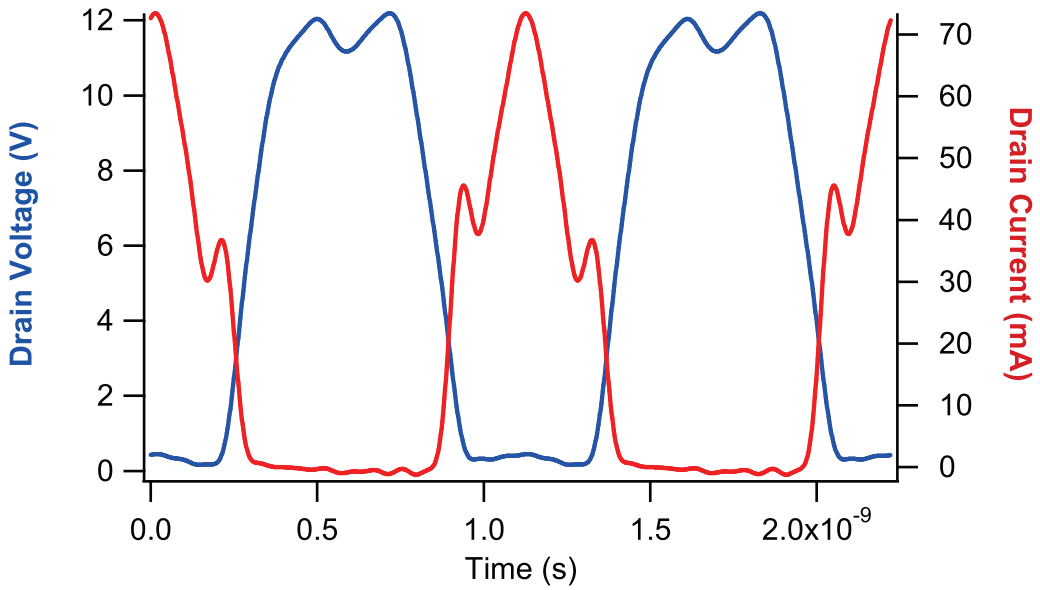








WaveForm Engineering – Why?



What are we looking for?

- Remember these waveforms exist at the internal node of the device so we are looking for zero current flowing when there is voltage and zero voltage flow when there is current.

$$P = V \times I$$

- The optimum harmonic loads are high (total) reflect as we are trying to confine the power delivered to the outside load only at the fundamental.

Limits to what is achievable -

- Control of a finite number of harmonic impedances.
- Device boundary conditions. Knee voltage/current pinch-off
- f_{MAX}

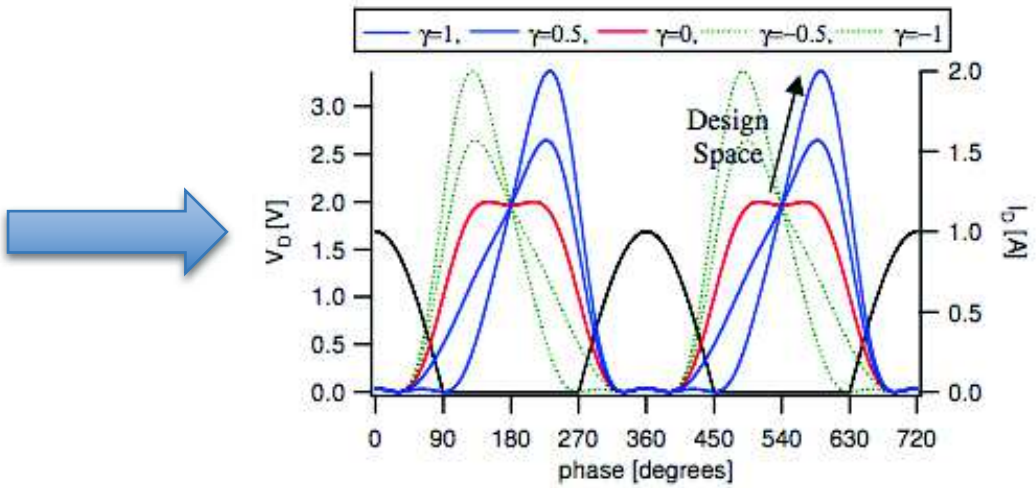
WaveForm Engineering – Why?

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- **I hit my optimum efficiency by manual tuning so who cares?**

1. Using the waveforms gets you there quicker
2. Did you get to the best possible solution?
3. How do you know you found the mode of operation you wanted too?

Recent discovery of continuous modes shows that there are an infinite number of F0 and 2F0 impedance combinations for a certain mode – Each voltage waveform shown yields same efficiency of 90.7%



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Worked Example - Measurement Time

F0 Load Points = 30

Power Points = 15

2F0 Load Points = 18

3F0 Load Points = 18

Frequencies = 3

Bias Points =3

Total Measurements = 30x15x18x18x3x3

= 1,312,200

Measurement time = 3 seconds

Total measurement time = **45 days!**

This could be reduced through appropriate modeling of the device and through improvements to measurement architectures or more intelligent decisions on measurement space

* see later presentations

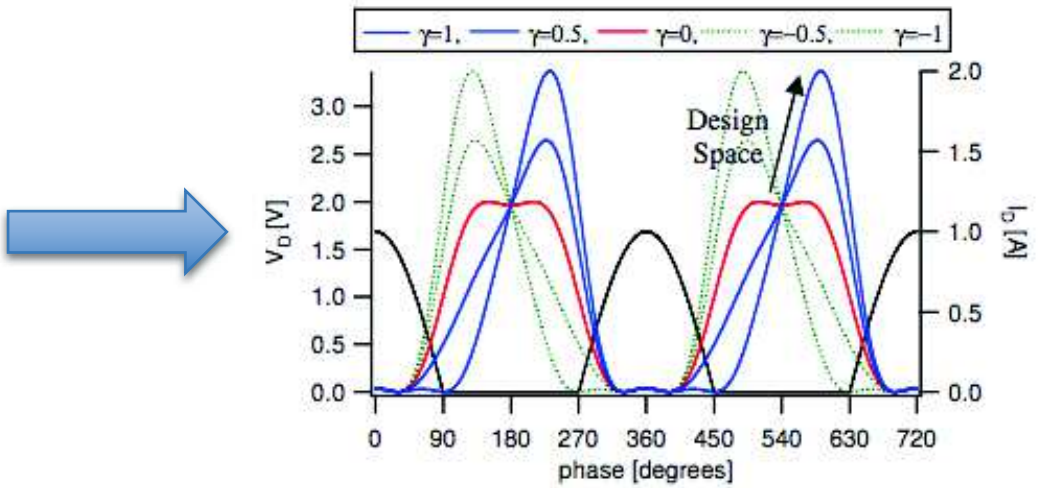
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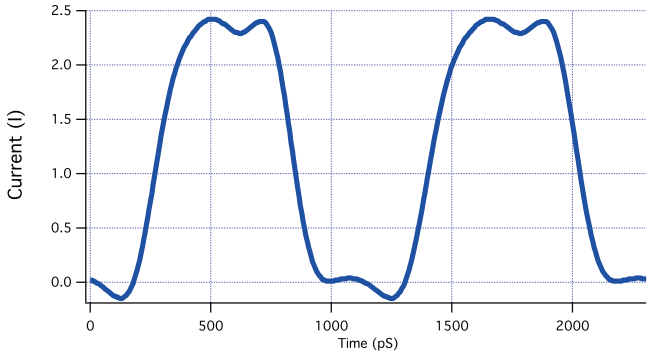
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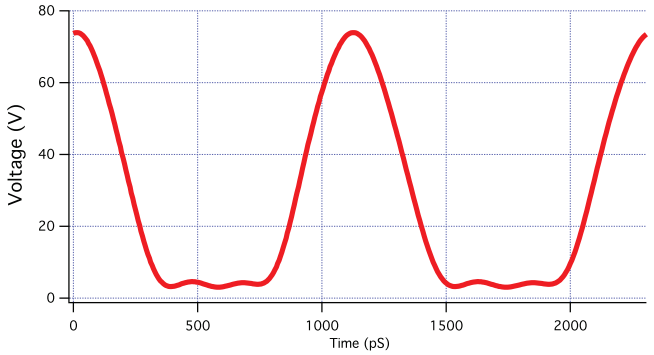


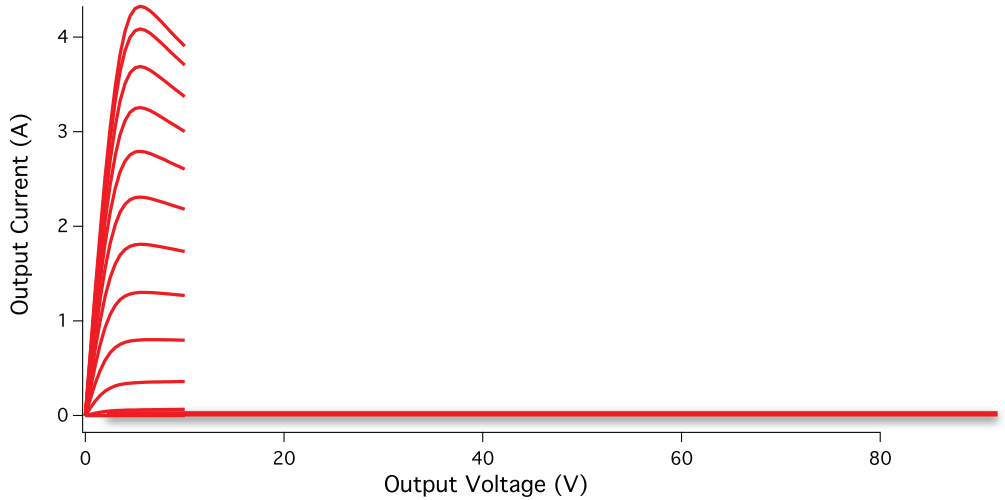
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WaveForm Engineering – Why?

- Comparing RF performance back to static device boundaries

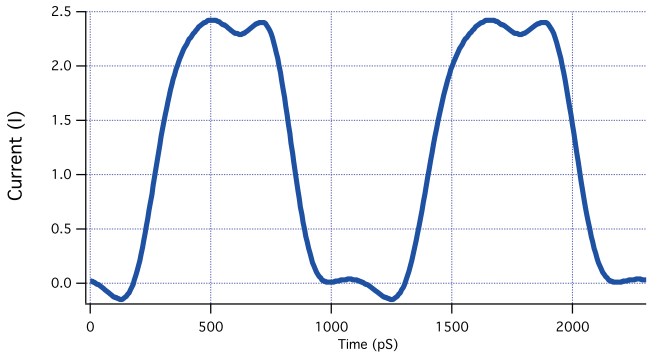




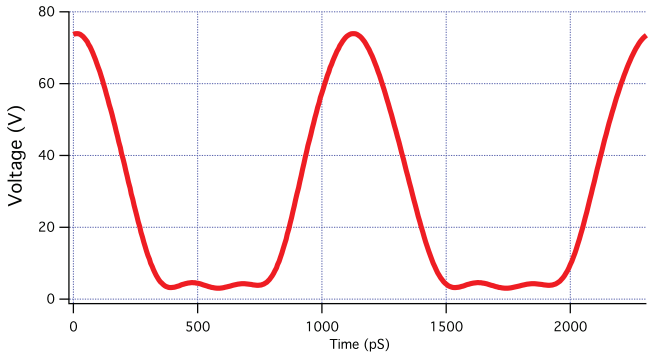


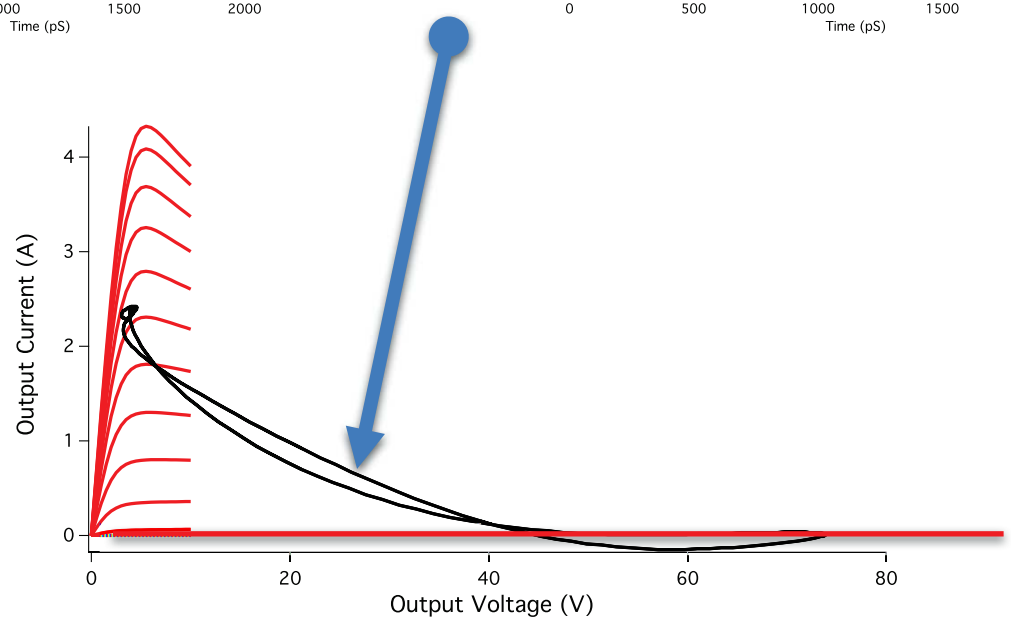
WaveForm Engineering – Why?

- Comparing RF performance back to static device boundaries



Vs.

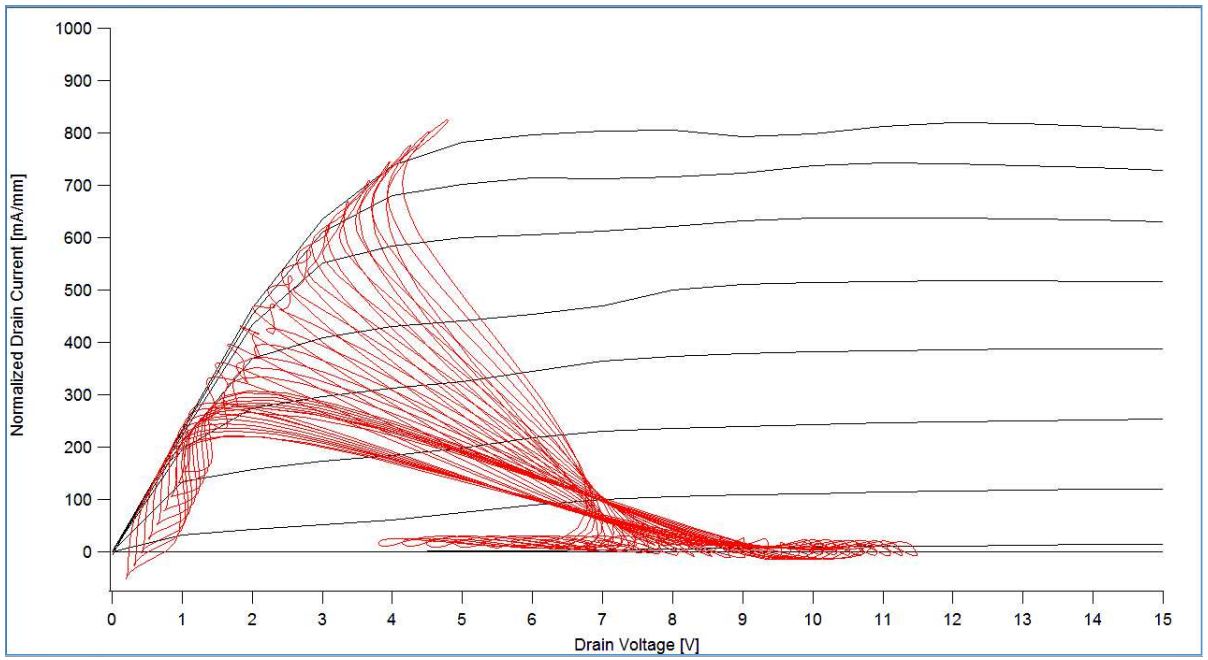




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WaveForm Engineering – Why?

- Comparing RF performance back to static device boundaries



Vary Impedance from low to high to map the RF knee of the device

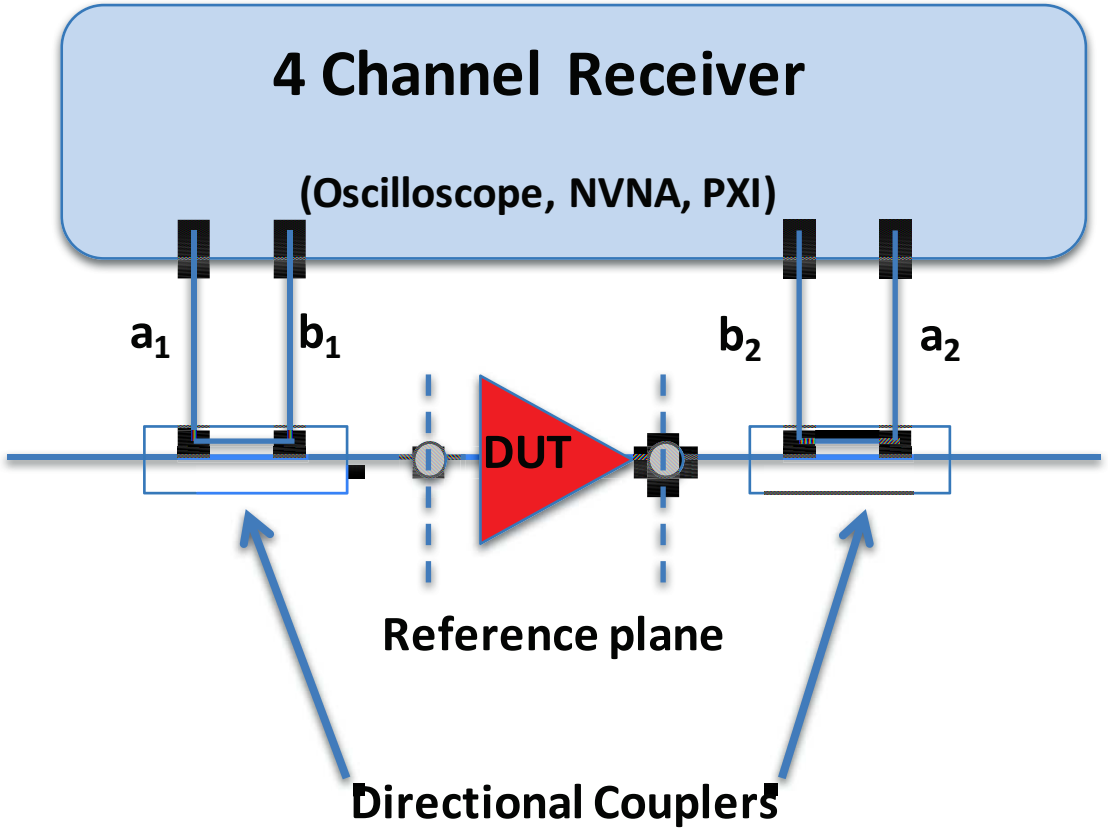
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Waveform Measurement

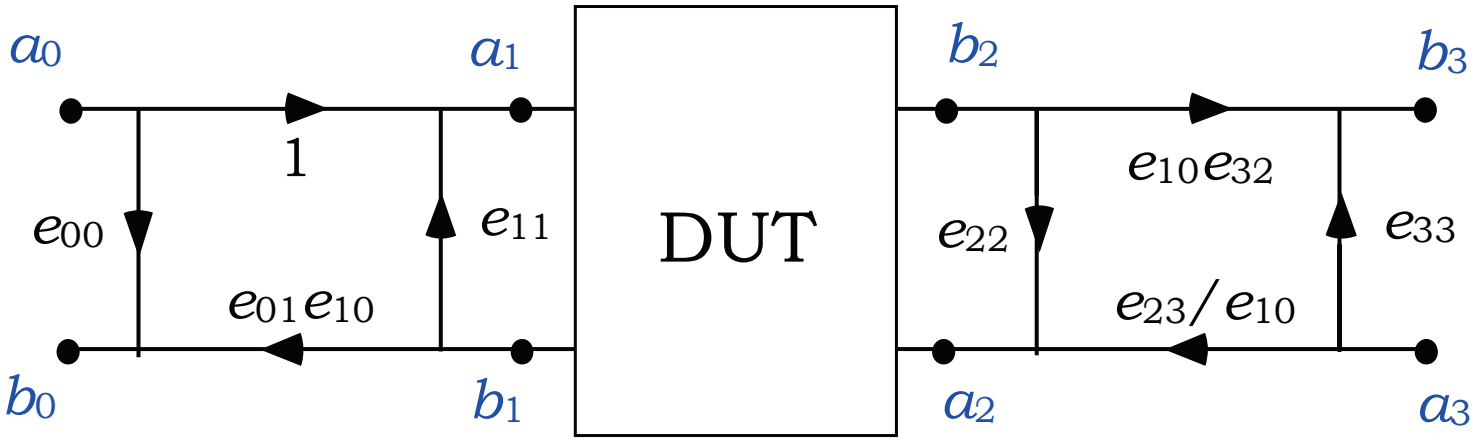
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WaveForm Engineering – Measurement



WaveForm Engineering – Calibration, Small Signal

- Standard small signal calibration, based on established techniques e.g TRL, SOLT etc.
- Based on Ratio measurements so end up with composite error terms, absolute measurements not possible.



WaveForm Engineering – Calibration, Absolute

- Absolute calibration involves reference to known standards in terms of power and phase.

- Power achieved with a calibrated power meter.

- Relative phase (time) either through reference standard (see next presentation) or implied through use of time domain oscilloscope.

- Finally connection of one of the ports either directly or via an extension calibration allows the composite terms to be split and a full error model of the system to be generated.

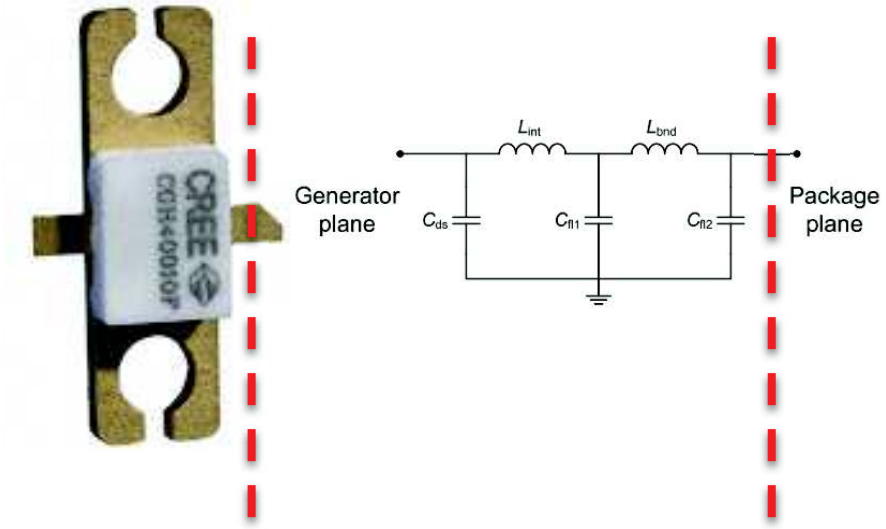
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De-Embedding for Waveform Measurement

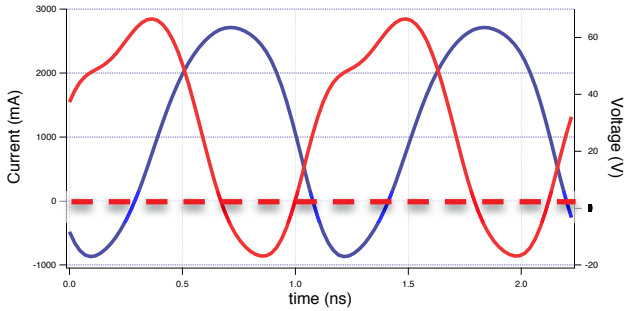
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WaveForm Engineering – De-embedding

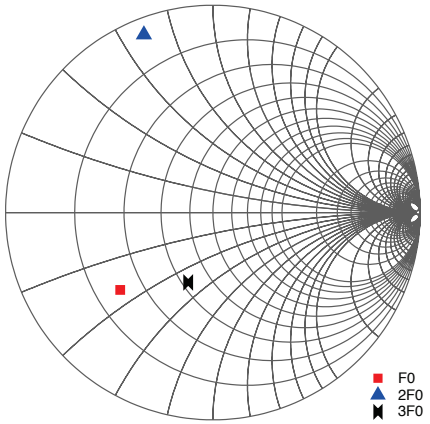
Not enough to measure waveforms need to de-embed to current generator for relation to device boundaries and power dissipation



Device Tabs



Waveforms



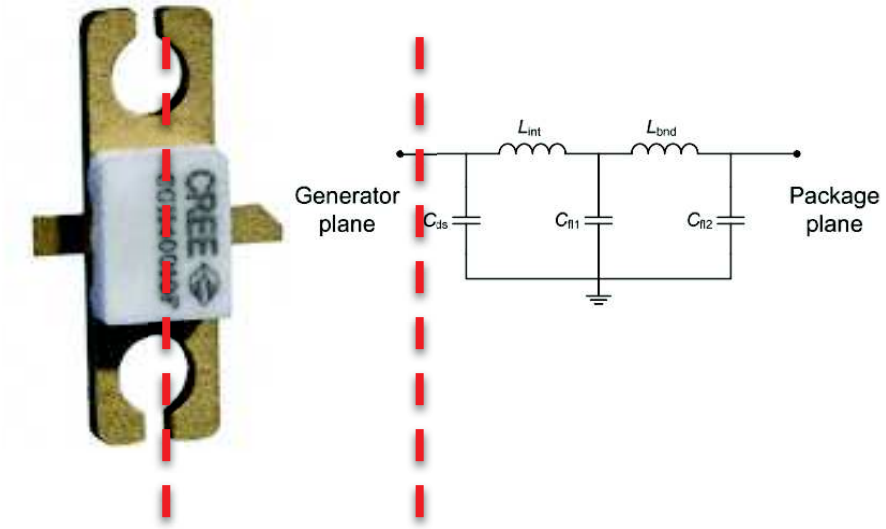
Impedance

Mesuro Software offers data display and impedance control at any reference plane, through upload of s-parameter files

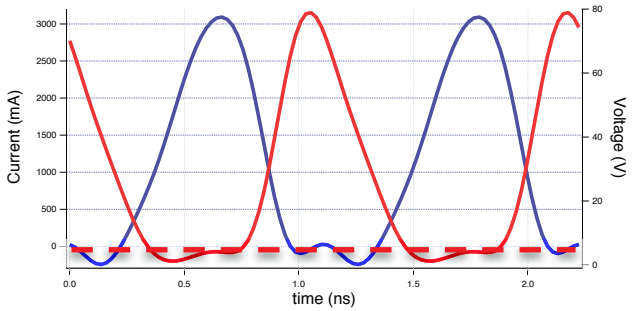
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WaveForm Engineering – De-embedding

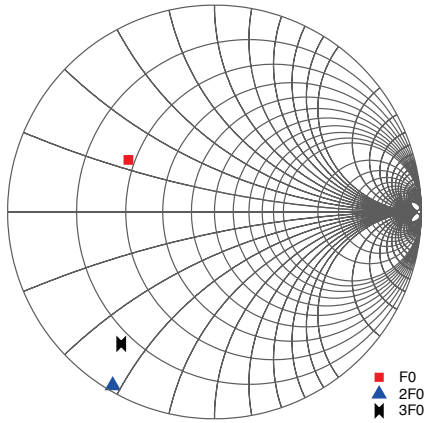
Not enough to measure waveforms need to de-embed to current generator for relation to device boundaries and power dissipation



Current Generator



Waveforms



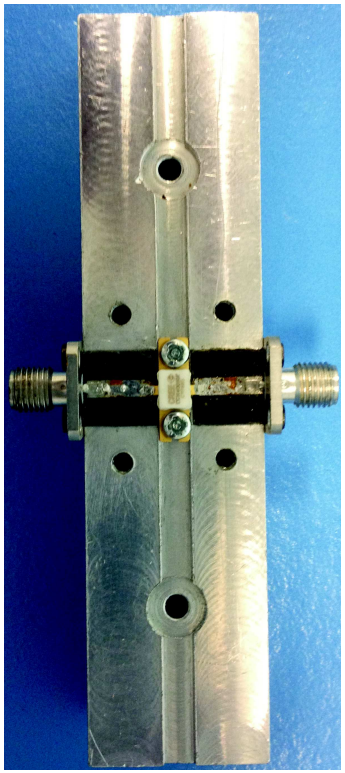
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WaveForm Engineering – De-embedding

- Important to understand the result of inaccuracies in your de-embedding network particularly in terms of which reference plane you are de-embedding to.
    - Where do I need absolute confidence?
    - Where can I start making assumptions?
    - What are you trying to de-embed?
        - On Wafer?
        - Packaged Device?
        - Full PA?



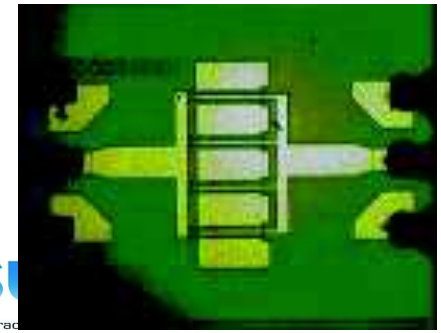
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WaveForm Engineering – De-embedding Approach

- **On wafer is cleanest environment!**

- Simplified model is good enough (typically only two elements), information required often available from manufacturers or in house. More complex extraction possible but not really necessary. Not necessary to model non-linear capacitance.

- Validation includes
  - Consistent interaction with boundary conditions of device.
  - Impedances for amplifier modes comply with theory.
  - Can change frequency with no effect on desired impedances.



WaveForm Engineering – De-embedding Approach

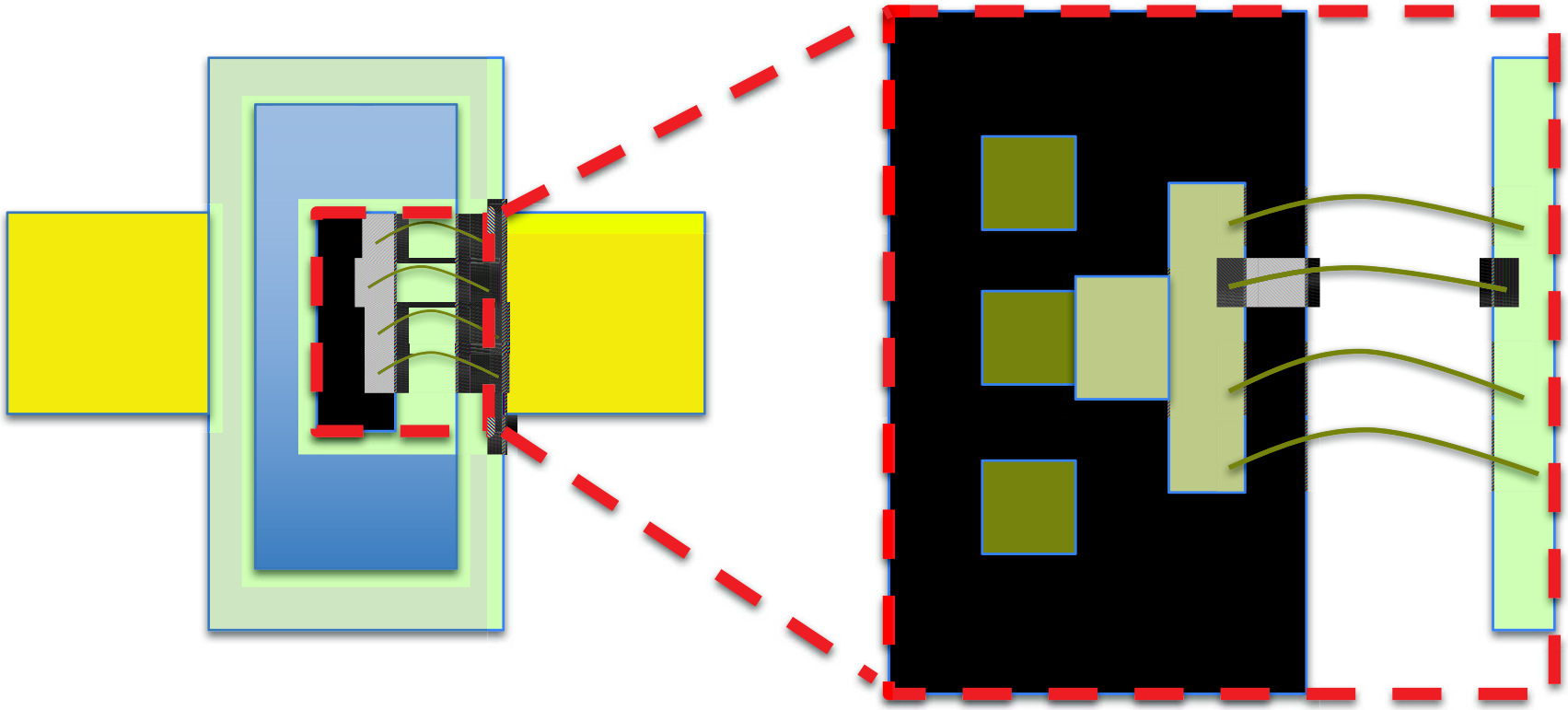
- **Package parasitics make life more difficult!**

- Model needs to become more complex, information from manufacturers not always available or accurate.

- Various Approaches can help
  - **Educated Guess!** Often this is sufficient. Similar package types have similar parasitics learn from experience – remove lids to gain information, number of bonds approximate length, size of pads etc.
  - **Forward and Reverse Bias Measurements** – Use forward measurement (short near I_{GEN}) to expose series inductances and reverse measurement (open near I_{GEN}) to expose shunt capacitances.
  - **Package models can be used** – down to availability and accuracy for application.

WaveForm Engineering – De-embedding Approach

- **If possible measure the package!** – lay probe pads down inside package, to allow measurement of the full 2-port s-parameters. Most accurate measurement.



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WaveForm Engineering – Waveform Shaping

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- Given the ability to measure voltage and current waveforms, the ability to de-embed back to the 'current generator'. To Engineer the waveform, need to be able to shape the voltage and current waveforms.

- The output current waveform can be shaped through a combination of input drive and bias. The voltage waveform is shaped by control of the fundamental and harmonic impedances presented to the device.
  - **This leads to a requirement for harmonic load-pull.**

V = I x R

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Waveform Shaping – Load-Pull

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WaveForm Shaping – Load-Pull Options

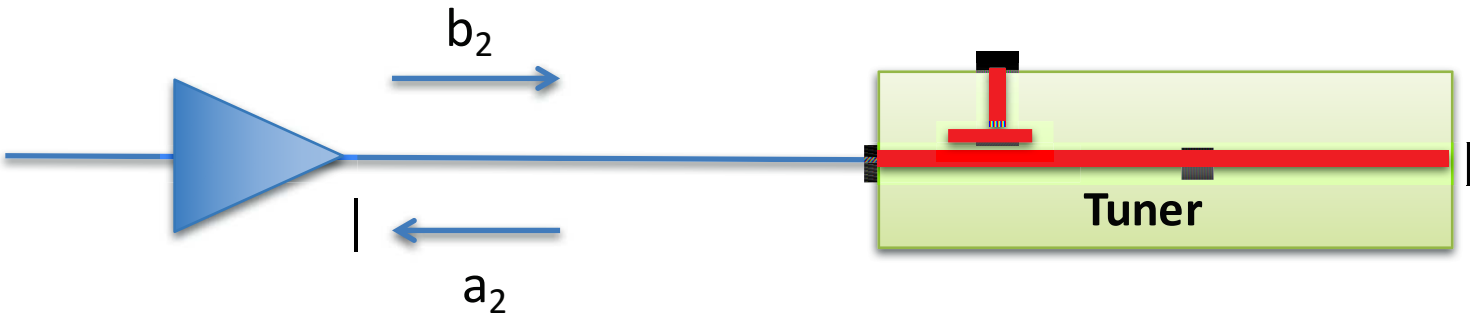
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Load-Pull – The control of the impedance environment around a device

- **Passive Load-Pull** – The output signal from the device is reflected of a passive network, changes to this passive network are used to vary the impedance environment.

- **Active Load-Pull**
  - **Closed Loop –** The device output is feed around a feedback loop, the magnitude and phase of the feedback signal are modified to vary the impedance environment.
  - **Open Loop –** The device output is terminated into a load, a new signal is electronically created to emulate the reflection of a load.

Load-Pull
- Passive Load-Pull



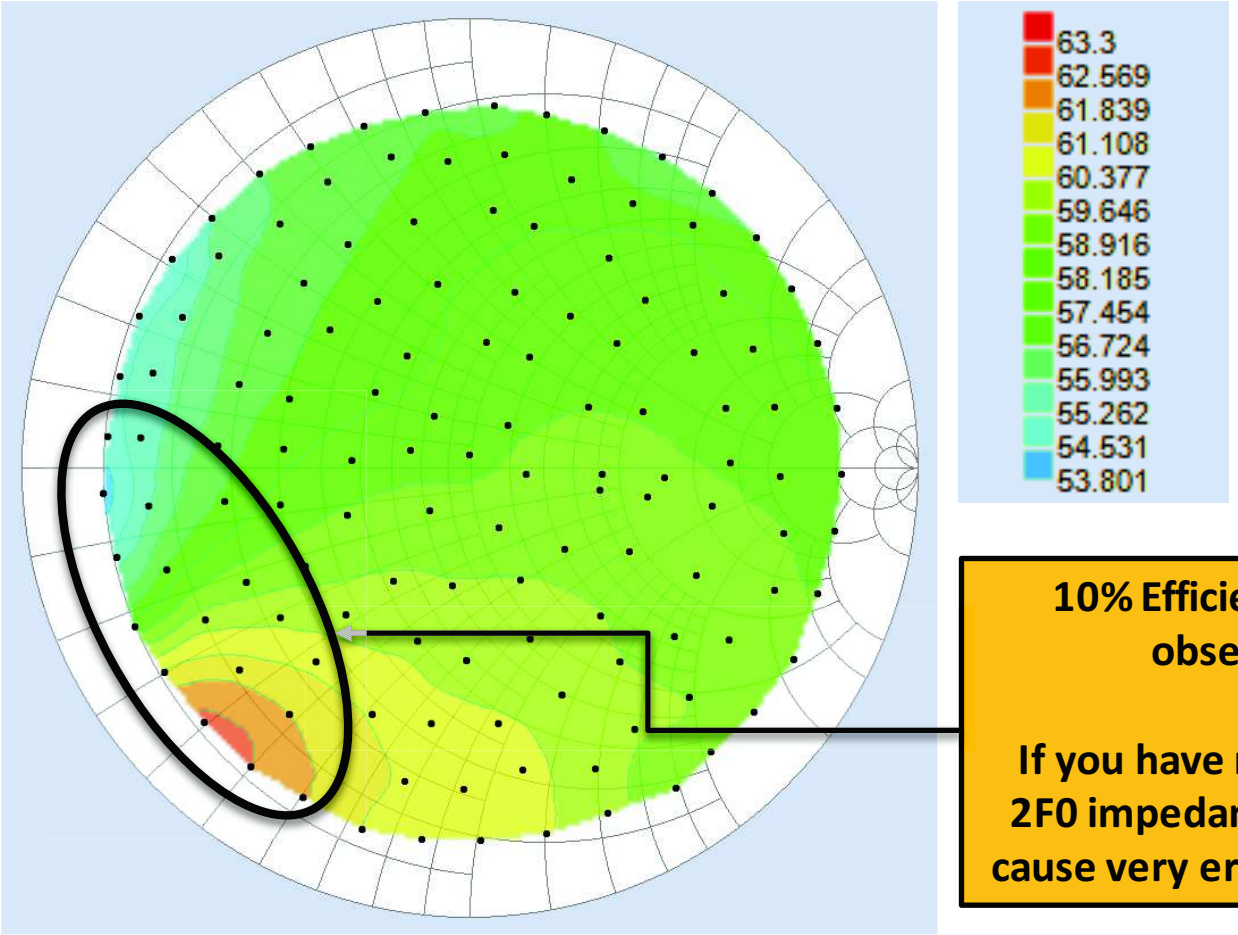
$$\Gamma = \frac{a_2}{b_2}$$

As long as it includes harmonics!!

Input and Output

Harmonic Source-pull Experimental Results (1)

Plot shows dramatic effect of 2F0 source impedance on measured efficiency



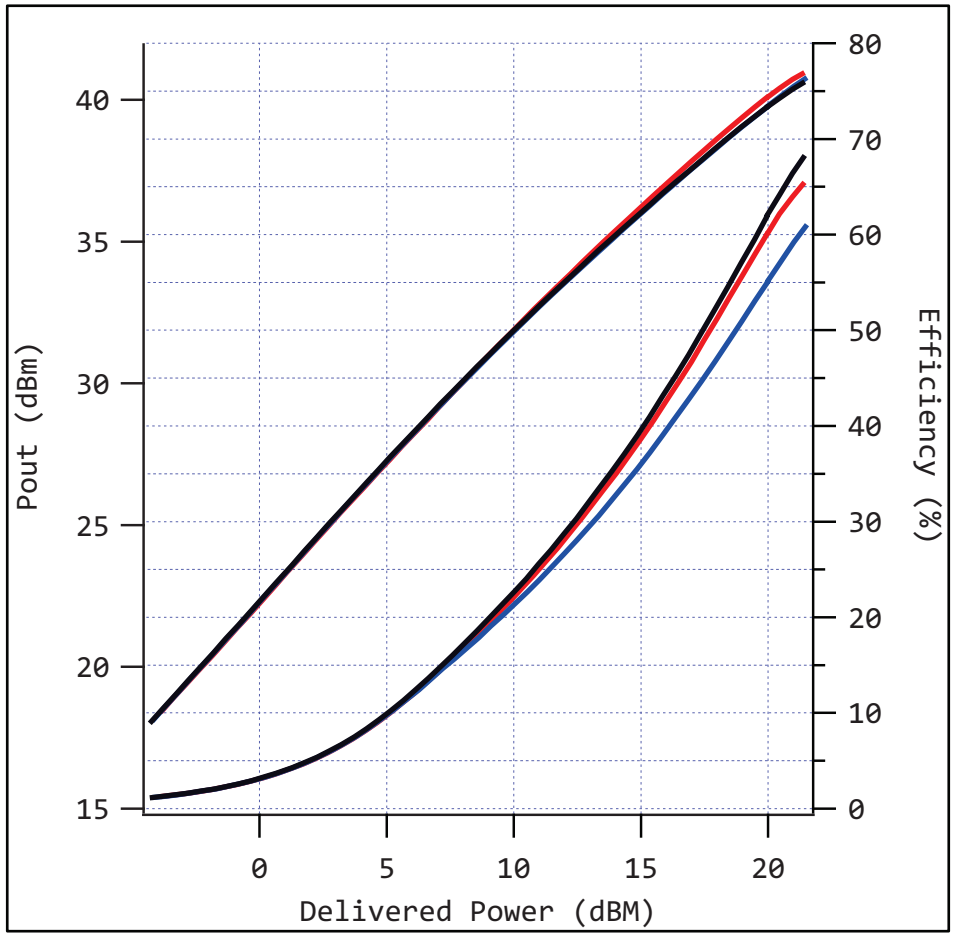
10% Efficiency swing observed!

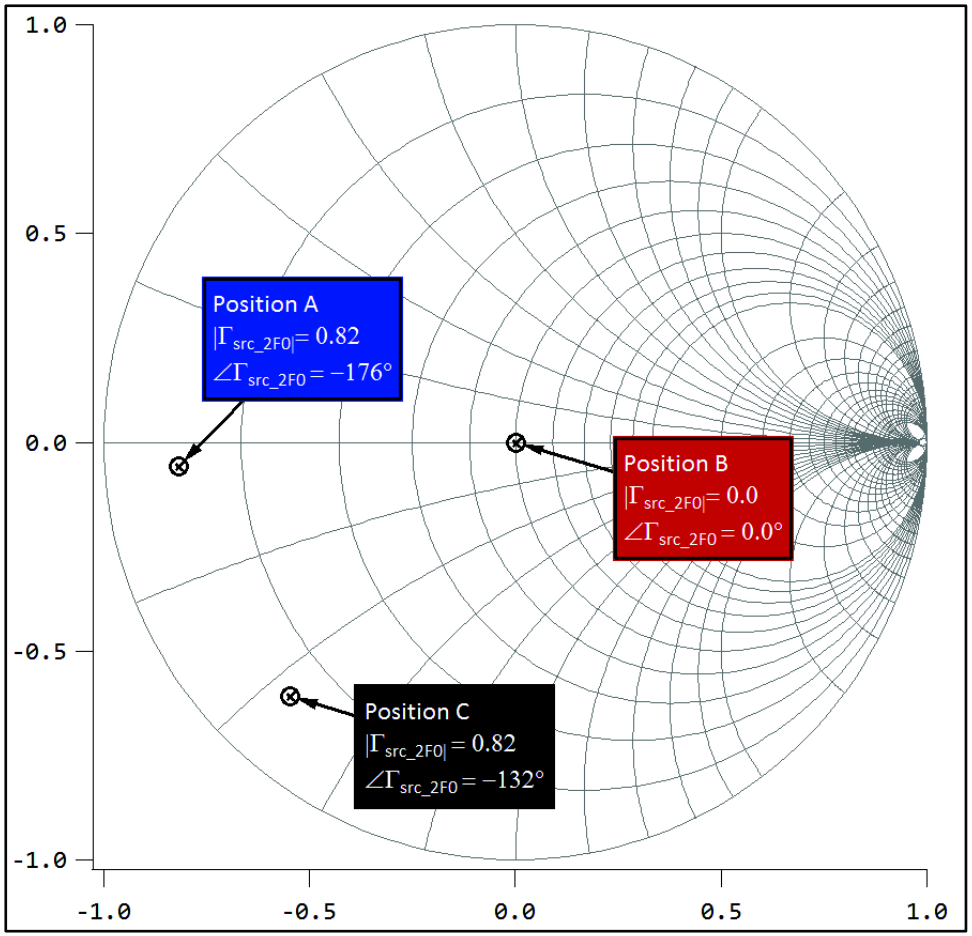
If you have no control of 2F0 impedance this could cause very erroneous data!

Harmonic Source-pull: Experiment Results (2)

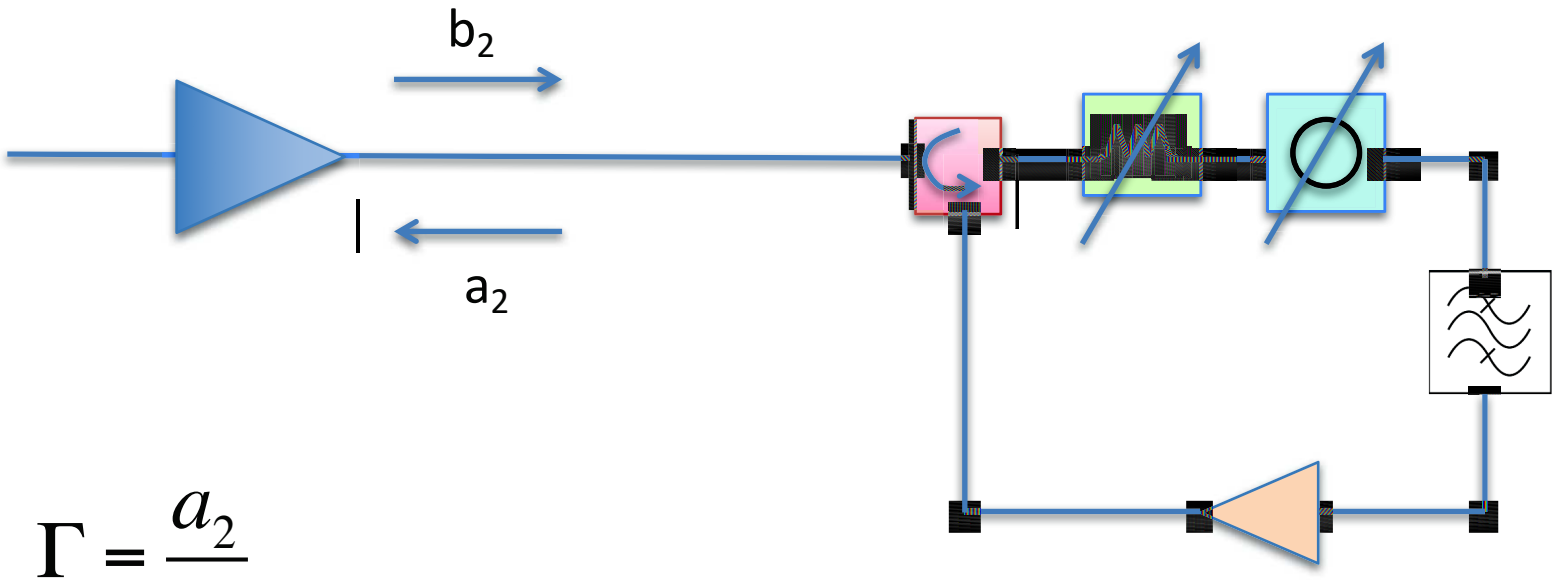
Plots show dramatic effect of 2F0 source impedance on measured power and efficiency.

All other parameters fixed as we move Source 2F0 between 3 states
(from 0<0 to 0.82<-176 to 0.82<-132)





Load-Pull
- Active Closed Loop



$$\Gamma = \frac{a_2}{b_2}$$



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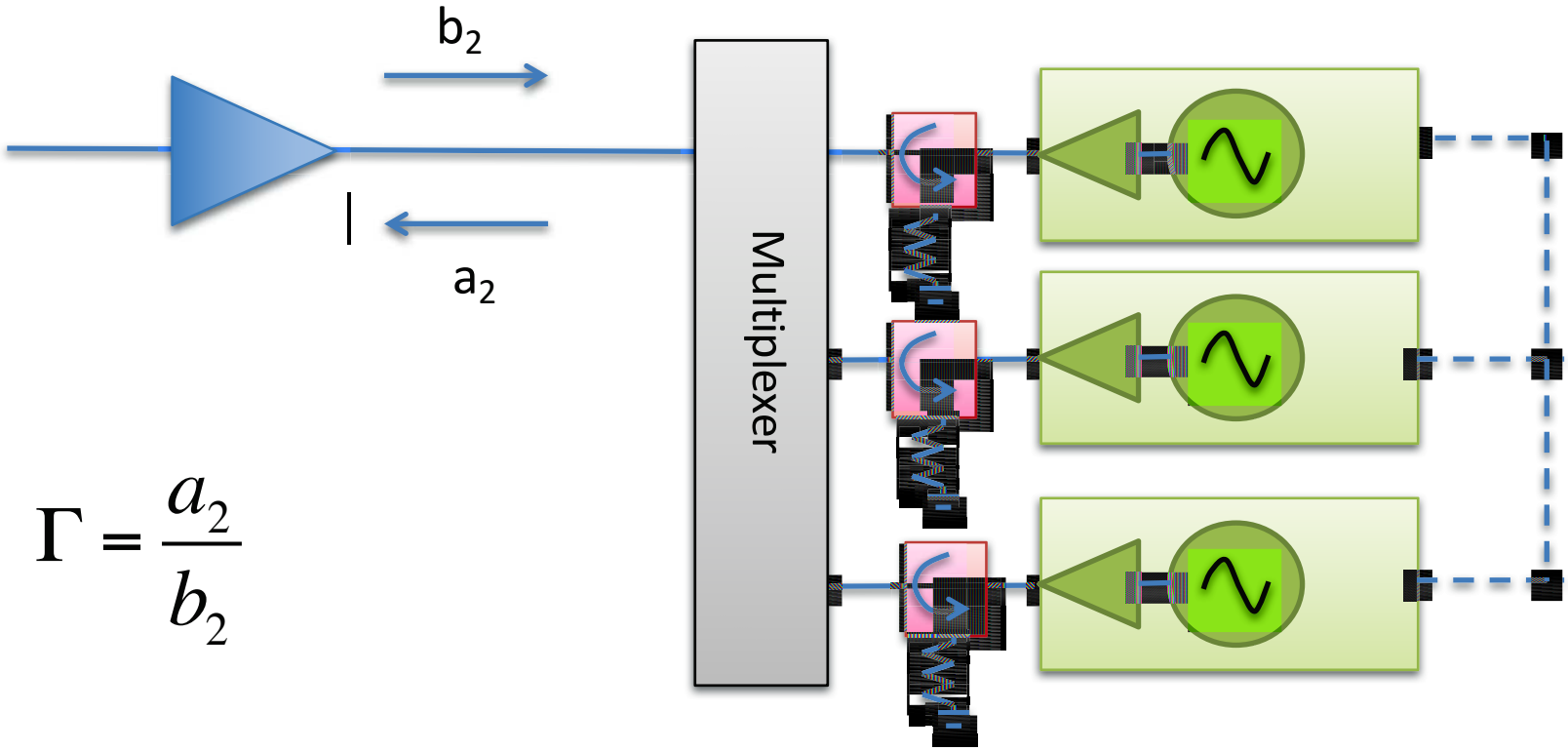
Load-Pull
- Active Open Loop



$$\Gamma = \frac{a_2}{b_2}$$

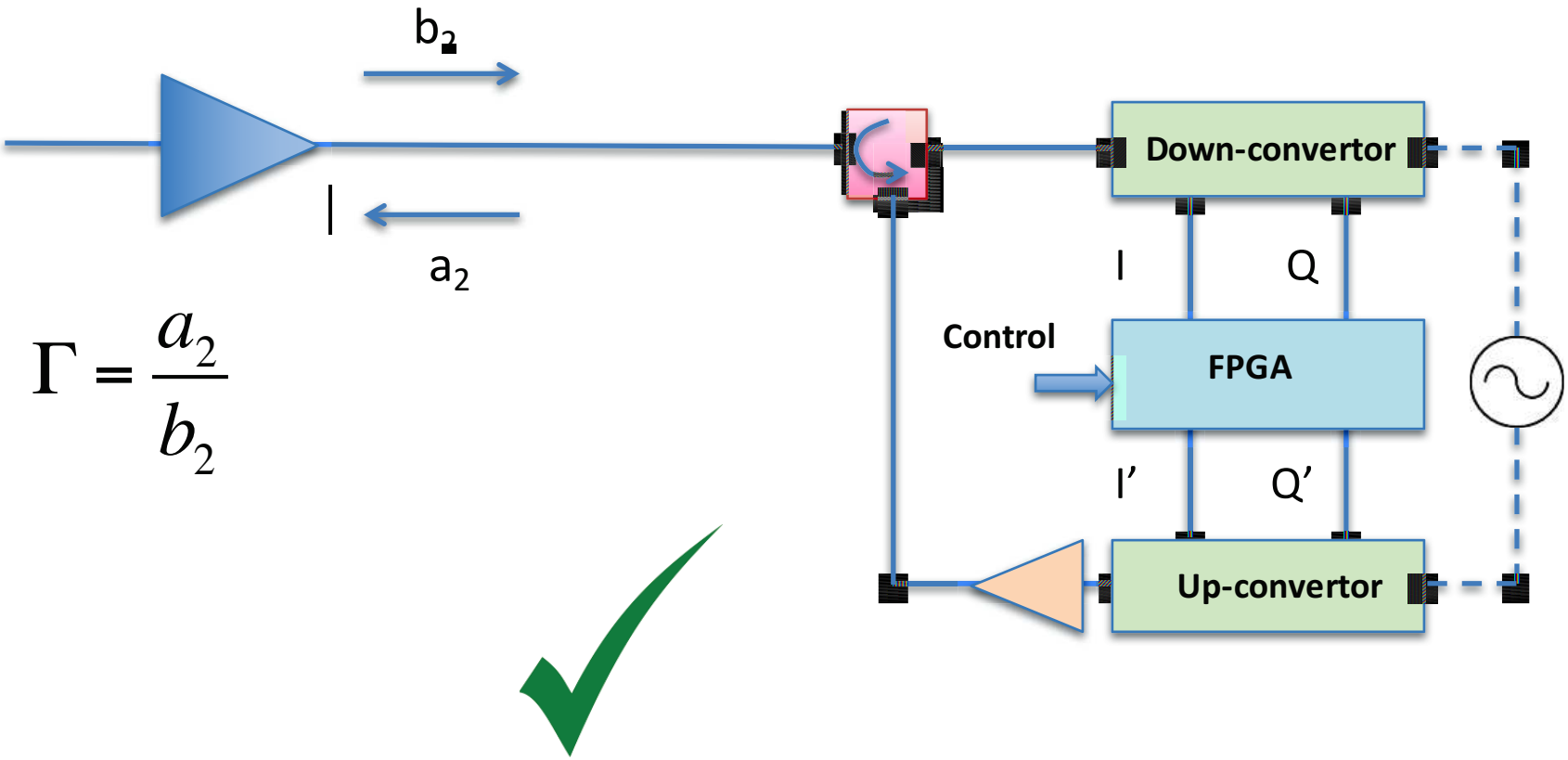


Load-Pull
- Active Open Loop



$$\Gamma = \frac{a_2}{b_2}$$

RAPID Digital Load-Pull

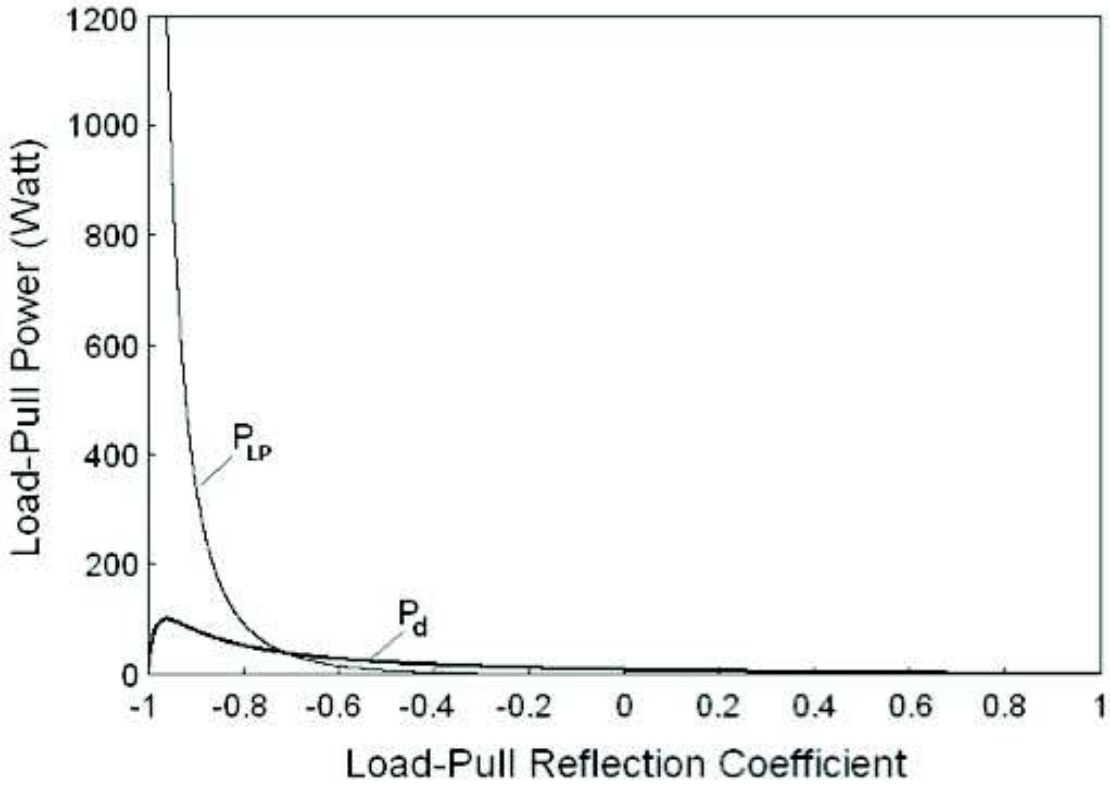


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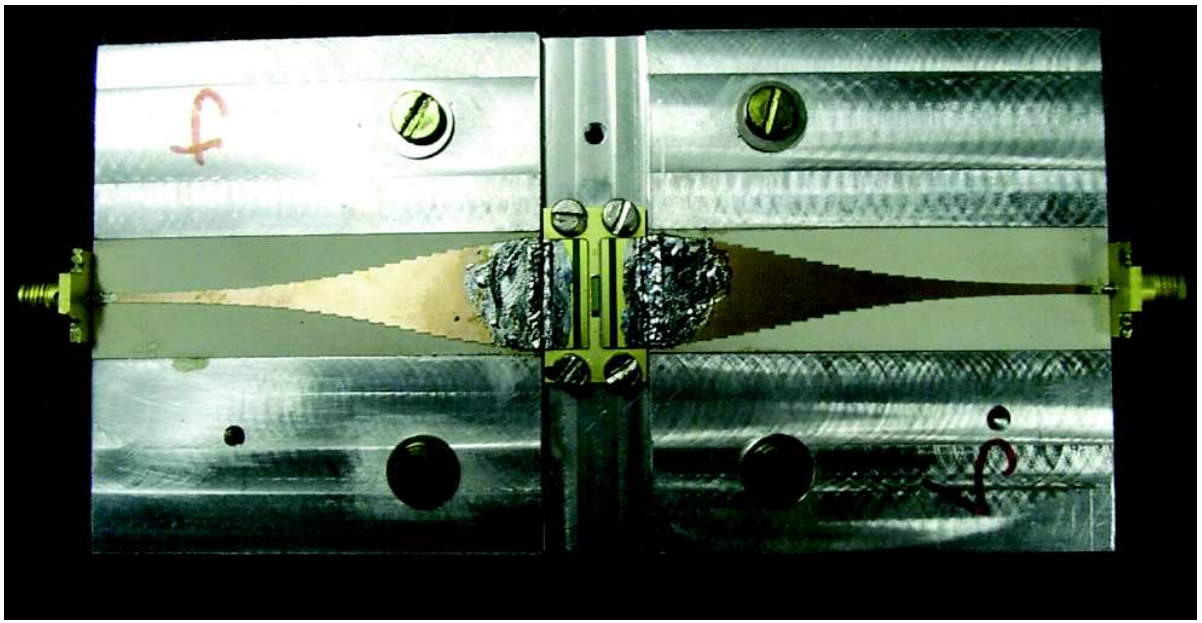
Active Load Pull At High Power

- Customers considering active load-pull are often concerned about the requirement of the system amplifiers

- If we look at the problem mathematically we can see that high power, low impedance devices require large amounts of power!

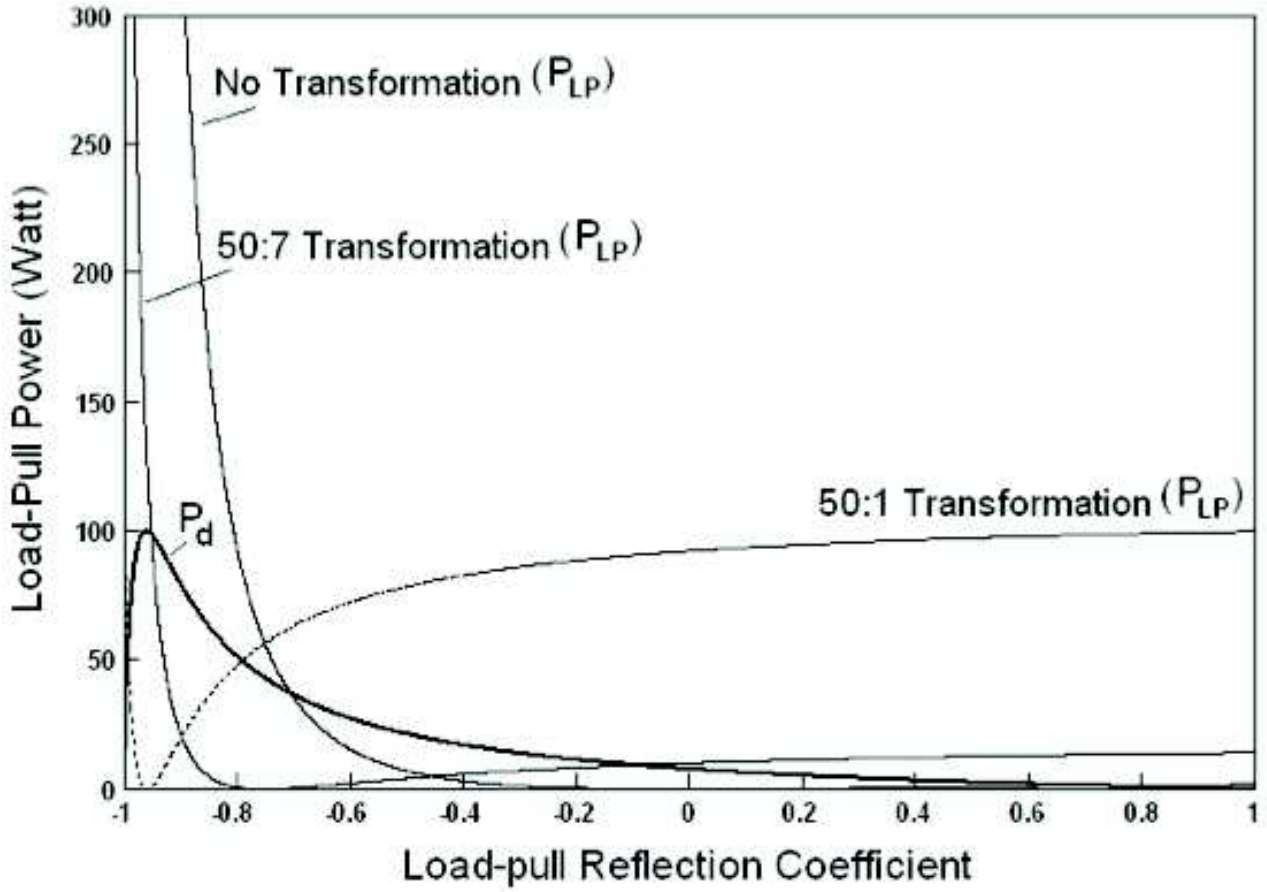


Active Load Pull At High Power

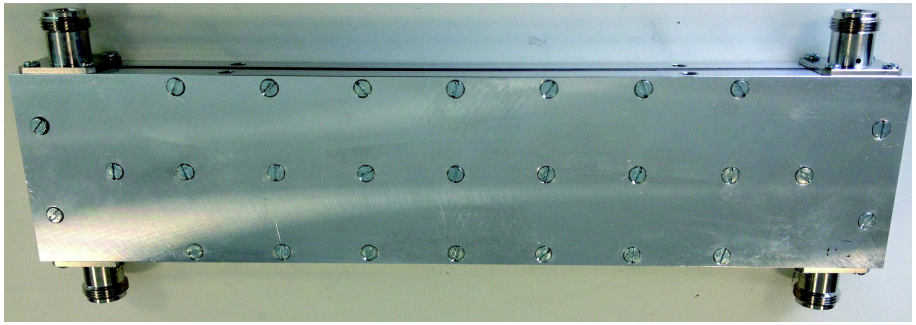


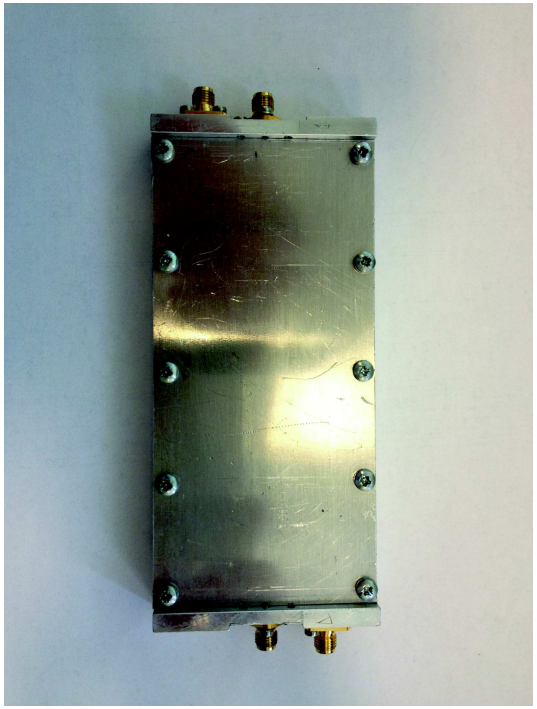
- The solution is to use wide-band impedance transformers to change the reference impedance of the measurement system. Very wide band coverage (100MHz to 12GHz has been demonstrated)

Active Load Pull
At High Power



Active Load Pull At High Power

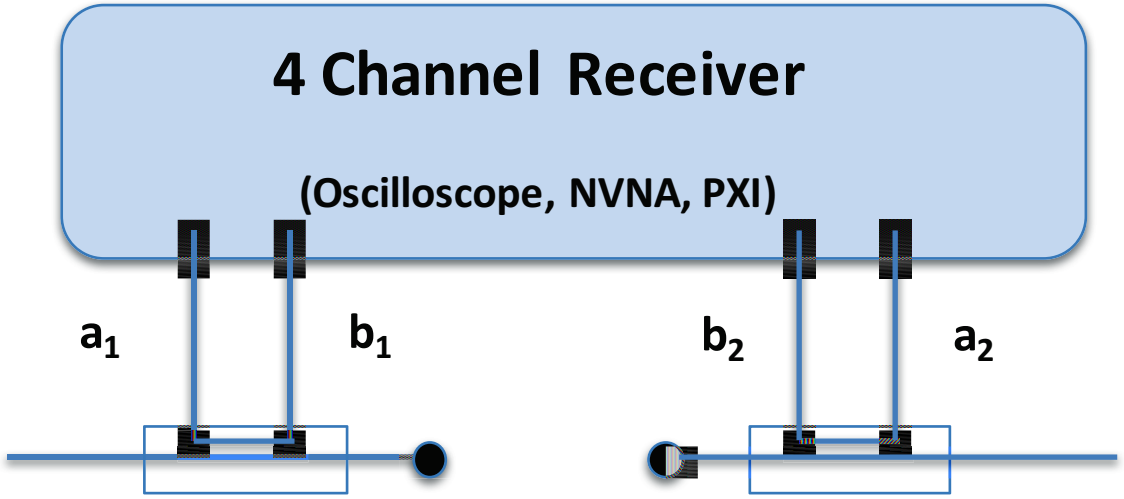




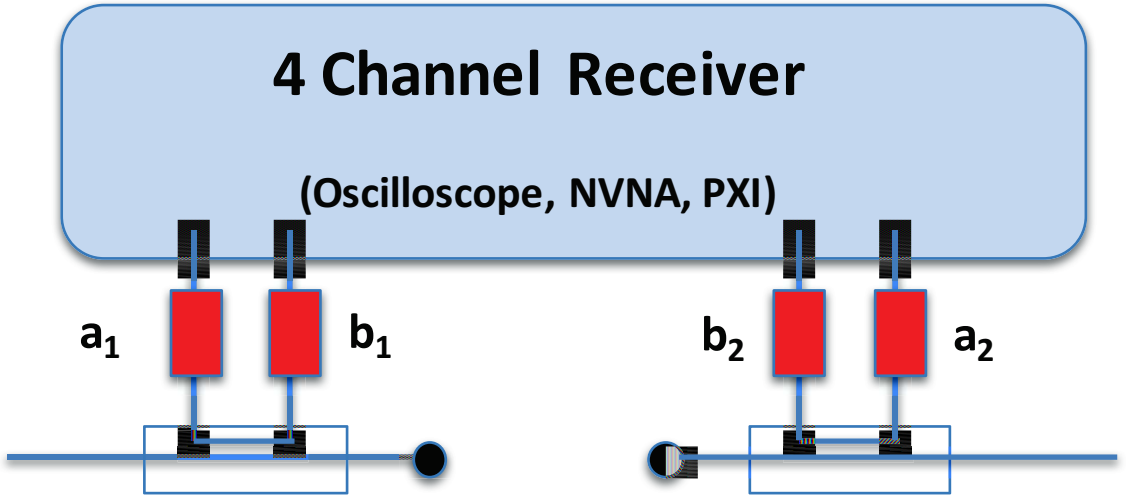
- Mesuro have developed and manufacture their own in-house components that are very suited to high power measurements.

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Active Load Pull
At High Power



Active Load Pull At High Power



- Scaling the receiver to high power can easily be achieved through the use of attenuators in the coupled lines, this leads to problems in calibration due to limited dynamic range.
- Solved in the Mesuro software as the user can de-embed from the measurements using s-parameter files.

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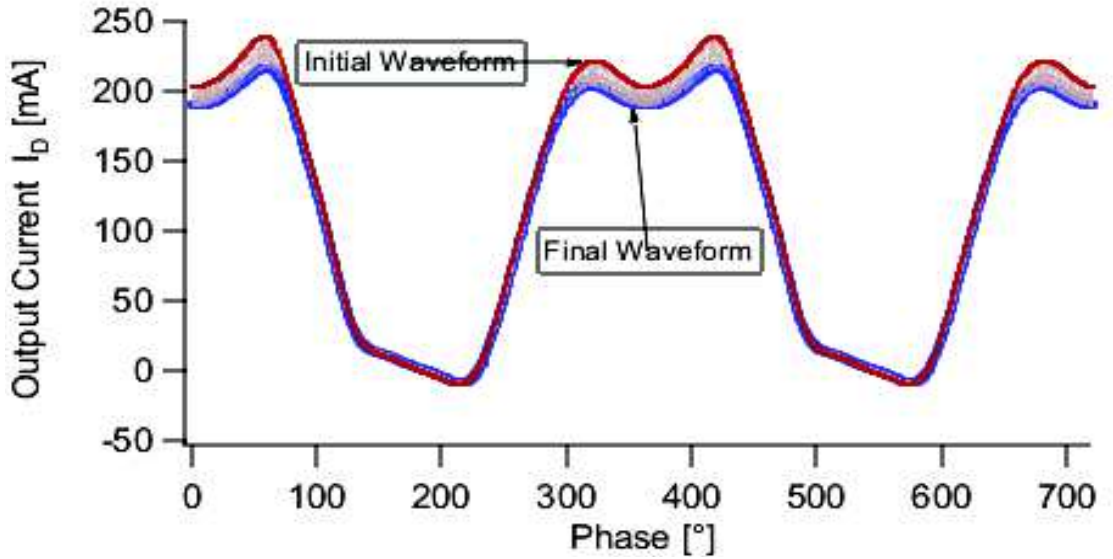
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Case Study 1 – Device Degradation

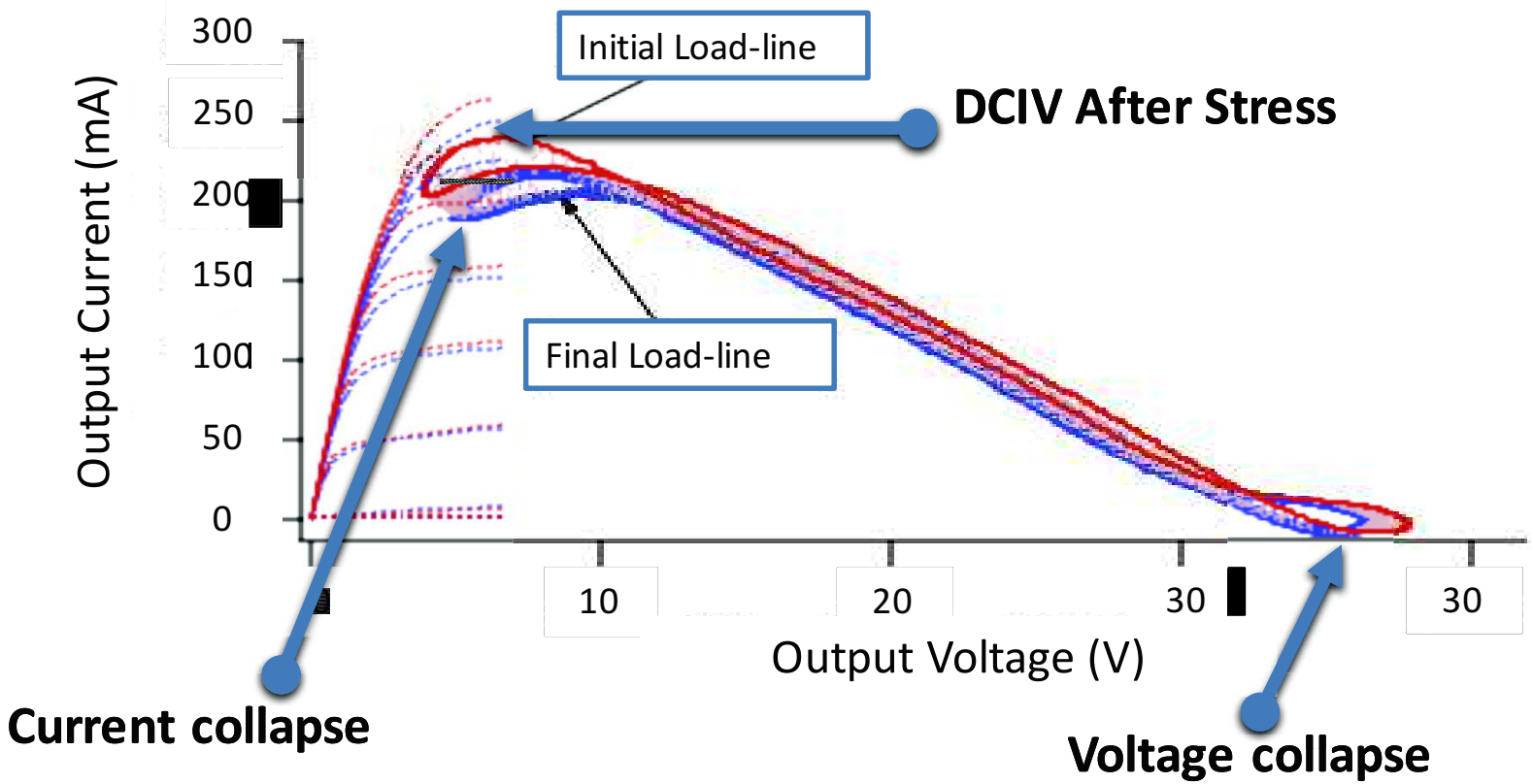
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Case Study
Device Degradation

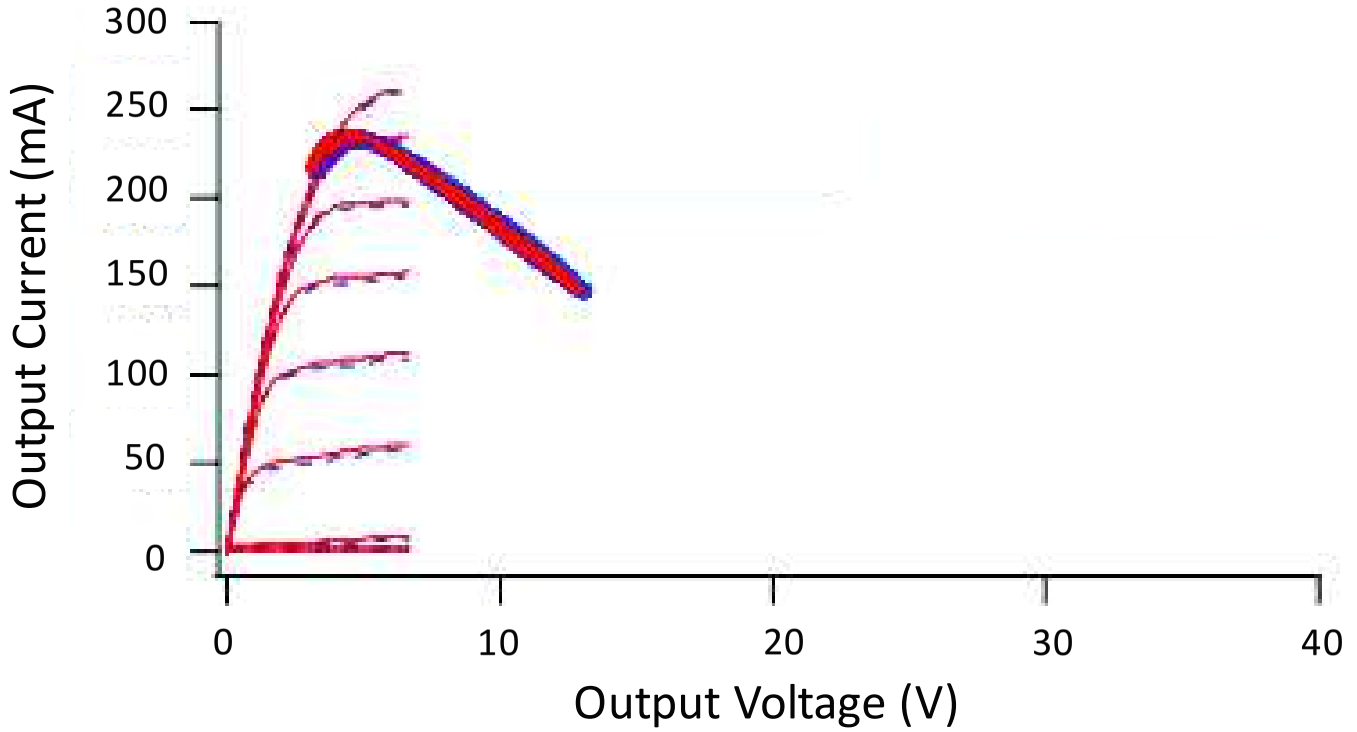
- Device held under static conditions.
- Clear degradation in power/efficiency over time.
- Waveforms showed reduction in peak current.



Case Study
Device Degradation

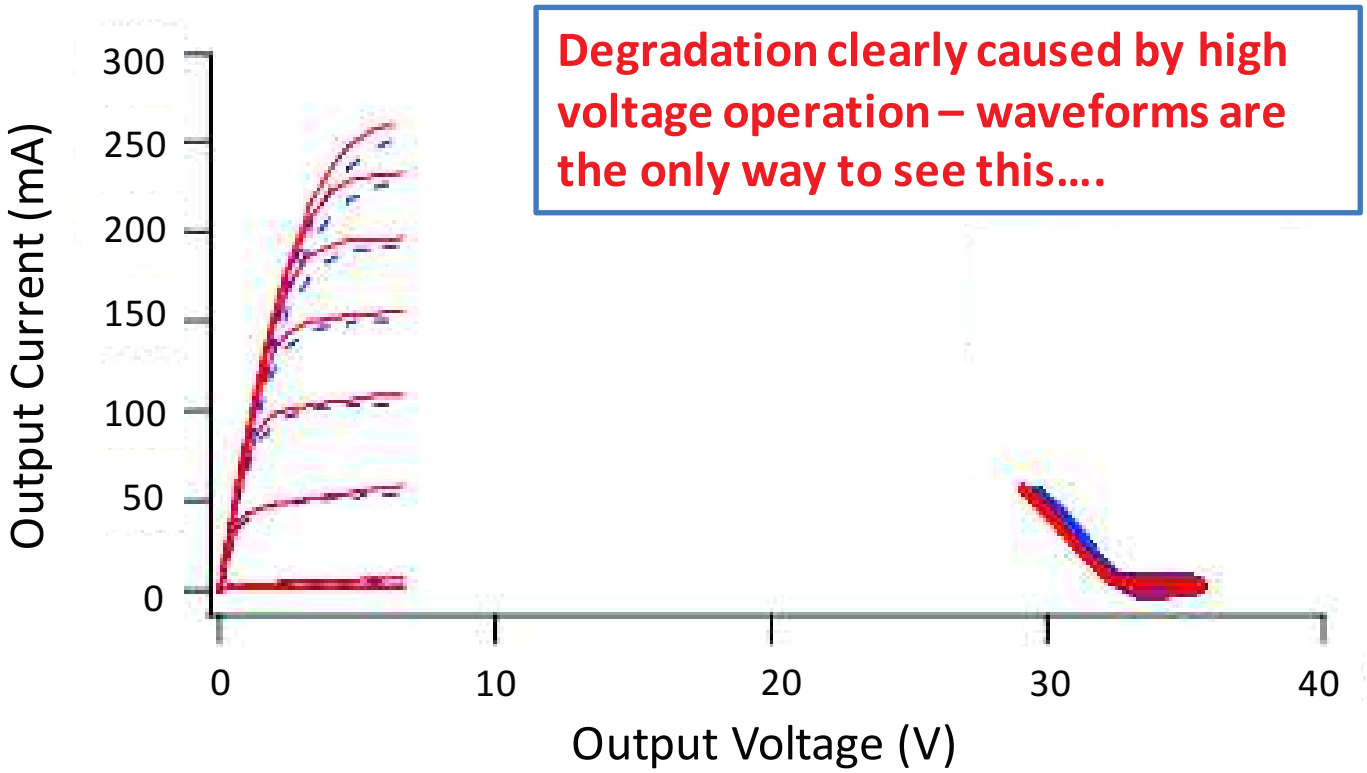


Case Study
Device Degradation



- Bias and drive used to limit load line to high current region of the I-V
- No Degradation in the IV post stress……

Case Study
Device Degradation



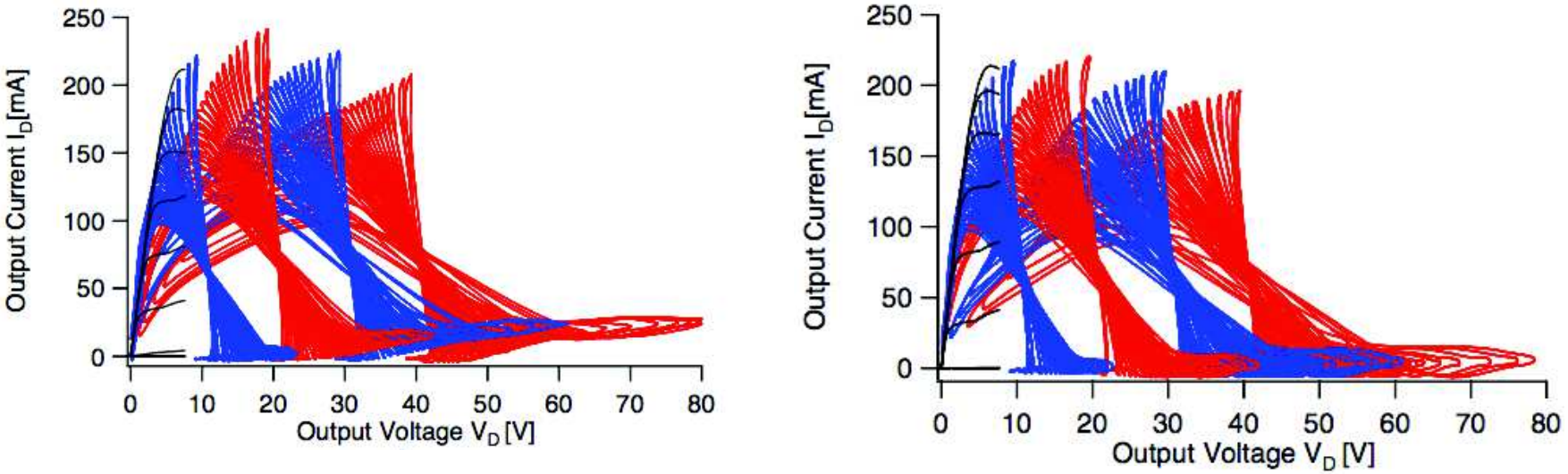
- Bias and drive used to limit load line to high voltage region of the I-V
- Clear Degradation in the DCIV post stress……

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Case Study 2 – Technology Development

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Case Study
Technology Development



Increased FE doping of buffer layer

- Early stage GaN device, significant knee walk out and soft pinch off problems.
- Access to dynamic RF performance allows manufacturer to focus efforts of a particular issue and make sure other performance is not degraded.

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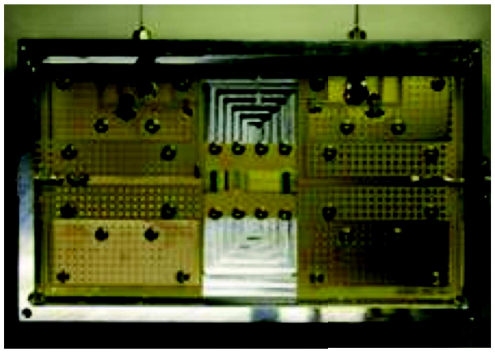
Case Study 3 – First Pass Design Success

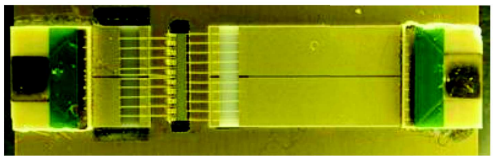
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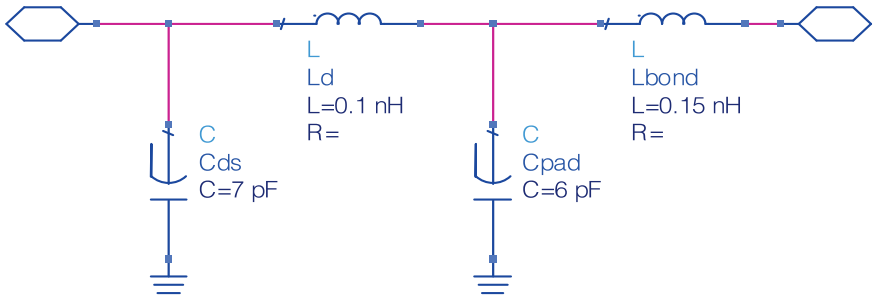
Case Study
First Pass Design Success

- First Pass Design of a 100W+, High Efficiency Class J GaN Amplifier

- Waveforms measurements conducted on an 80W HFET Device, with the aim of finding class J operation. Smaller device than final application chosen for thermal reasons.
- Successful de-embedding of fixture and device parasitics achieved







Reference – Iwata, M et al. 'First Pass Design of A High Power 145W, High Efficiency Class J Amplifier using Waveform Engineering.' – IEEE Radio and Wireless Week 2013.

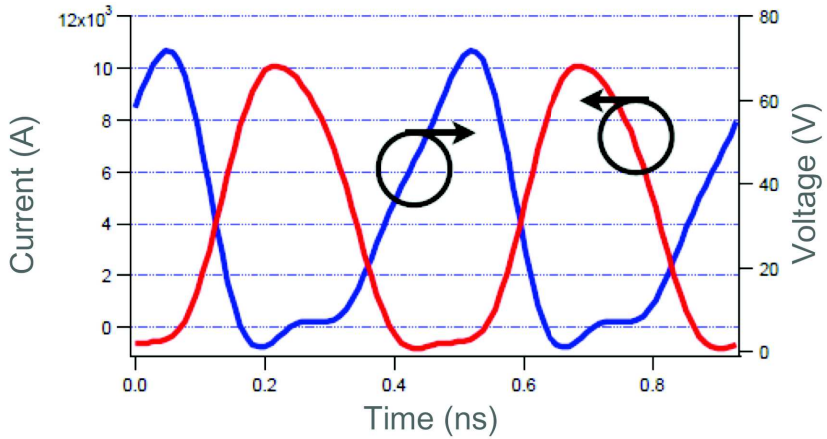
Panasonic Corporation

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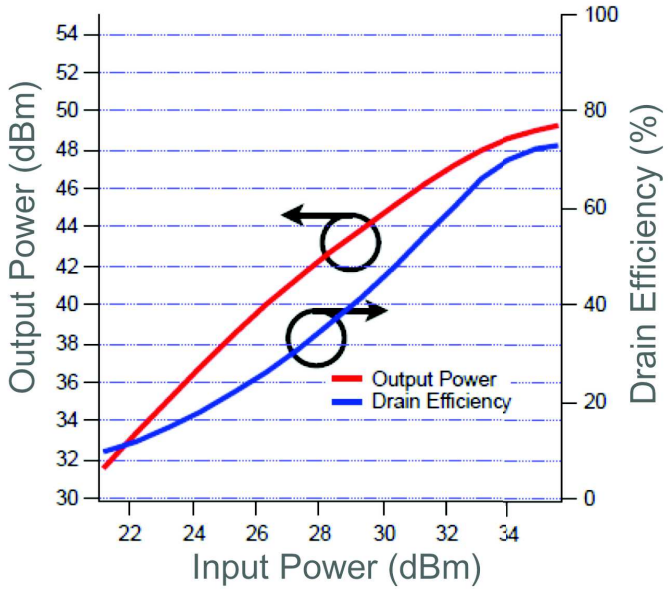
Case Study
First Pass Design Success

- First Pass Design of a 100W+, High Efficiency Class J GaN Amplifier

- Starting at theoretical class J impedances, second harmonic impedance tuned to optimise, waveforms and performance. Good class J waveforms – Impressive for a very high power device.



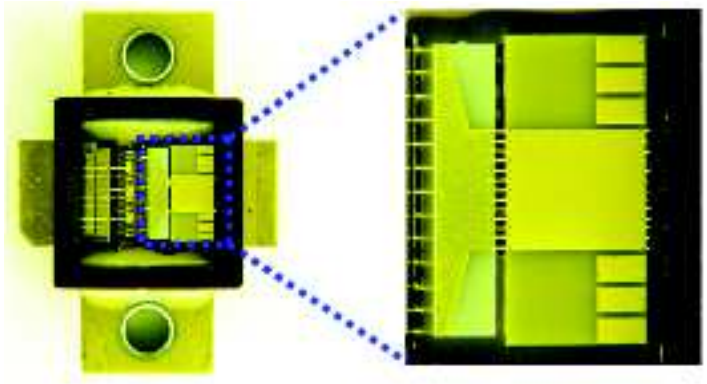
Mesuro/Panasonic measurements – 79W, 73.9% drain efficiency.



Case Study
First Pass Design Success

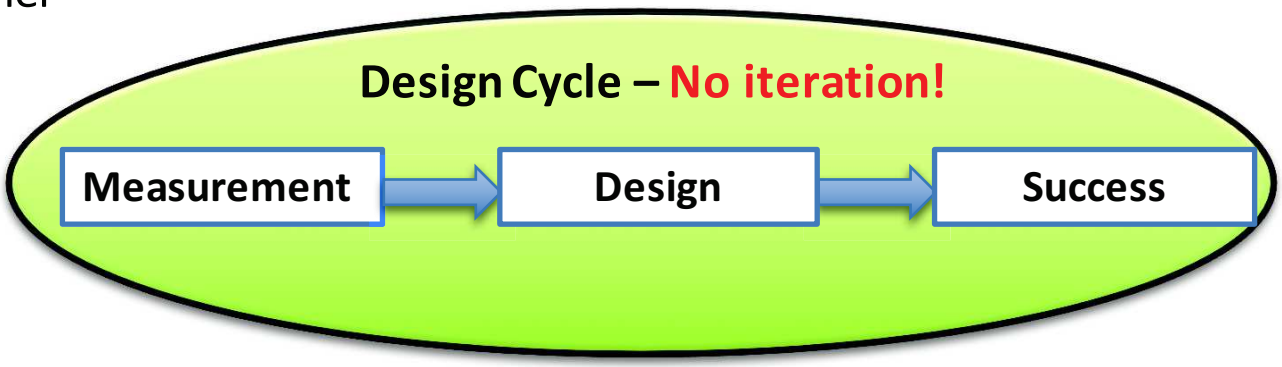
- First Pass Design of a 100W+, High Efficiency Class J GaN Amplifier

- Target was 70% drain efficiency, greater than 100W CW, device size therefore increased by 30%.



Realised Power Amplifier

Realized PA measurements –
Almost ideal scaling!
Efficiency of 71% at 105W
Only 2% reduction in efficiency from system measurements. Likely to be caused by matching loss.



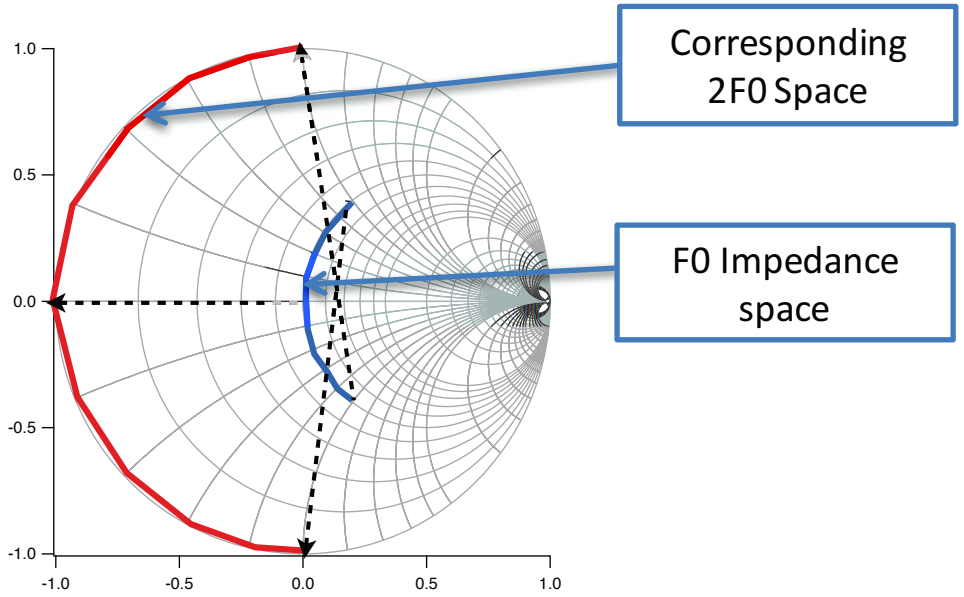
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Case Study 4 – Wide-Band Amplifier Design

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Case Study
Wide-Band Amplifier Design

- Until quite recently high efficiency modes of operation were applicable only to narrow band (<10% bandwidth) due to requirement of high Q resonators. Enhanced understanding of continuous modes have yielded very wide band high efficiency design.

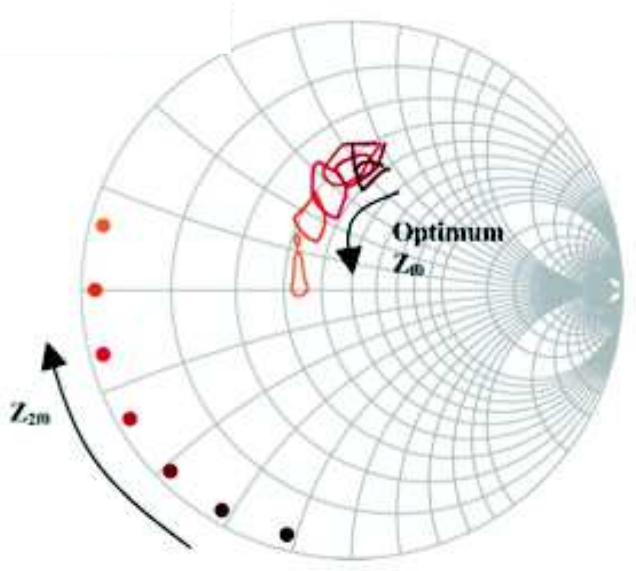


Normalized class B-J impedances – pairs of F0 and 2F0 loads that all give the same theoretical 78% efficiency performance at constant output power

Offers a moving target, easier to hit over frequency.

Not a compressed mode of operation so can be quite linear.

Case Study
Wide-Band Amplifier Design

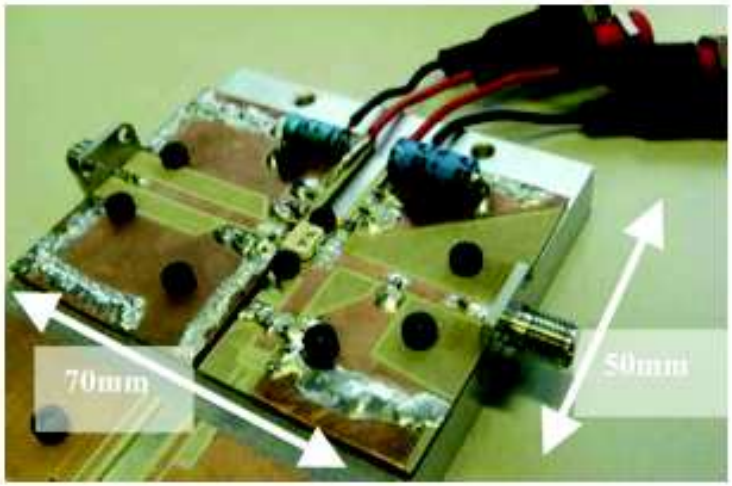


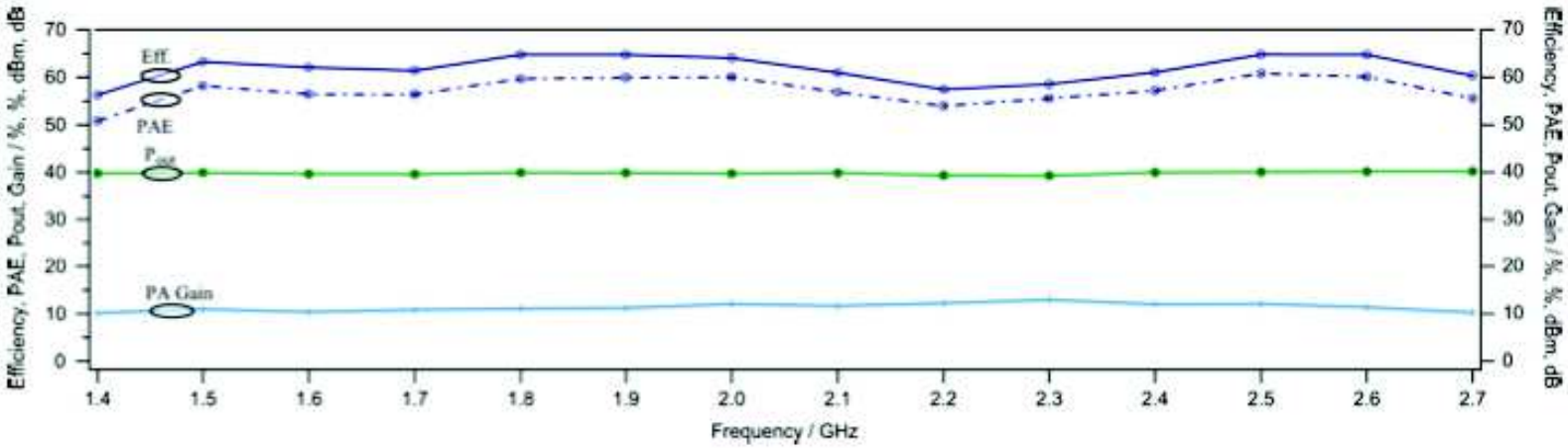
Measurements of fundamental efficiency contour (top 2%) for different 2F0 loads

Reference – Wright, P et al. 'A Methodology for Realizing High Efficiency Class-J in Linear and Broadband PA' – IEEE Transactions on Microwave Theory and Techniques VOL. 57, No 12, December 2009

Case Study
Wide-Band Amplifier Design

Realised PA design, very wide-band with >60% efficiency from 1.5-2.7GHz, almost flat power and gain profile





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Conclusions

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Conclusions

- Provided an Introduction to WaveForm Engineering
  - How to do Waveform Engineering
  - Why do Waveform Engineering?
- Case Studies
  - Process Development/Improvement
  - Amplifier Design

Waveforms truly let you see and understand your device from a new perspective!

- More Information Visit www.mesuro.com
- Contact tudorwilliams@mesuro.com

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Designing with Waveforms

Tutorial – High Efficiency Class F Amplifier

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Efficiency Expectations

- The achievable efficiency in a real power amplifier is constrained by the ability to correctly engineer the correct waveforms.
- The efficiency is governed by the ability to convert DC voltage and current into voltage and current components at the fundamental frequency in the RF waveforms.

$$\eta_{Voltage} = \frac{V_{RF}}{\sqrt{2 \times V_{DC}}}$$

$$\eta_{Current} = \frac{I_{RF}}{\sqrt{2 \times I_{DC}}}$$

$$\eta = \eta_{Voltage} \times \eta_{Current}$$

Efficiency Expectations Harmonic Limitations

- Assuming ideal waveforms it is possible to calculate the maximum possible efficiency in various modes of operation, the effect of limiting the number of terminated harmonic for Class F is also shown.

Class	$\eta_{Current}$	$\eta_{Voltage}$	η(%)
B	1.111	0.707	78.5
F	1.111	0.900	100
F (3 Harm)	1.111	0.816	90.6
F (4 Harm)	1.111	0.853	94.8
F (5Harm)	1.111	0.870	96.7

Typically 3 harmonics are used due to diminishing returns in real designs.

Efficiency Expectations Transfer Characteristic

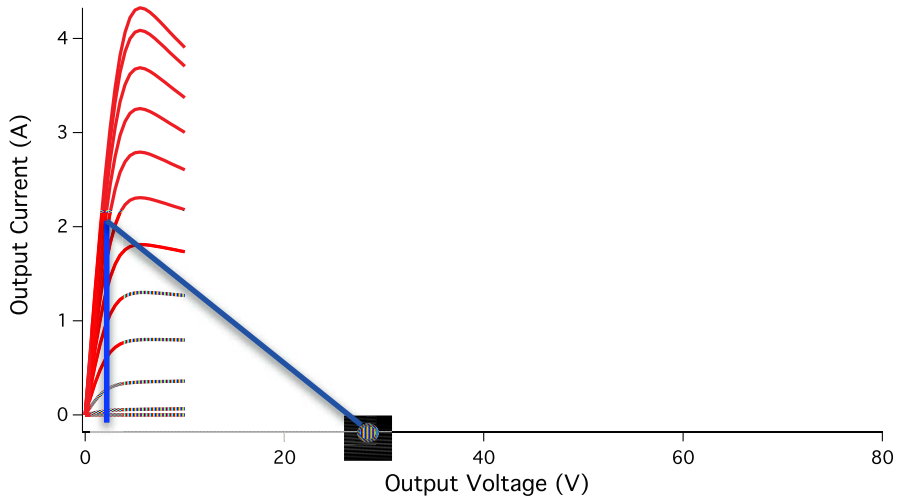
- A significant limitation in practical designs comes from the transfer characteristic which makes a fraction of the DC power unavailable for conversion to RF power -

$$\eta_{Offset} = \left(1 - \frac{V_{Min}}{V_{DC}}\right)\left(1 - \frac{I_{Min}}{I_{DC}}\right)$$

$$\eta = \left(\eta_{Current}\right)\left(\eta_{Voltage}\right)\left(\eta_{Offset}\right) \times 100$$

Efficiency Expectations Transfer Characteristic

- Remember that the knee – is not just governed by the DC performance, need to take account of Knee walkout, current collapse and pinch-off problems if present!



DCIV for 28V GaN device shown, note that the effect of the knee also impacts the peak current (power density) you are aiming for from the device.

Rule of thumb – anything more than 10% of V_D begins to seriously effect efficiency.

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Efficiency Expectations
Modes of Operation

- Assuming ideal waveforms it is possible to calculate the maximum possible efficiency in various common modes of operation -

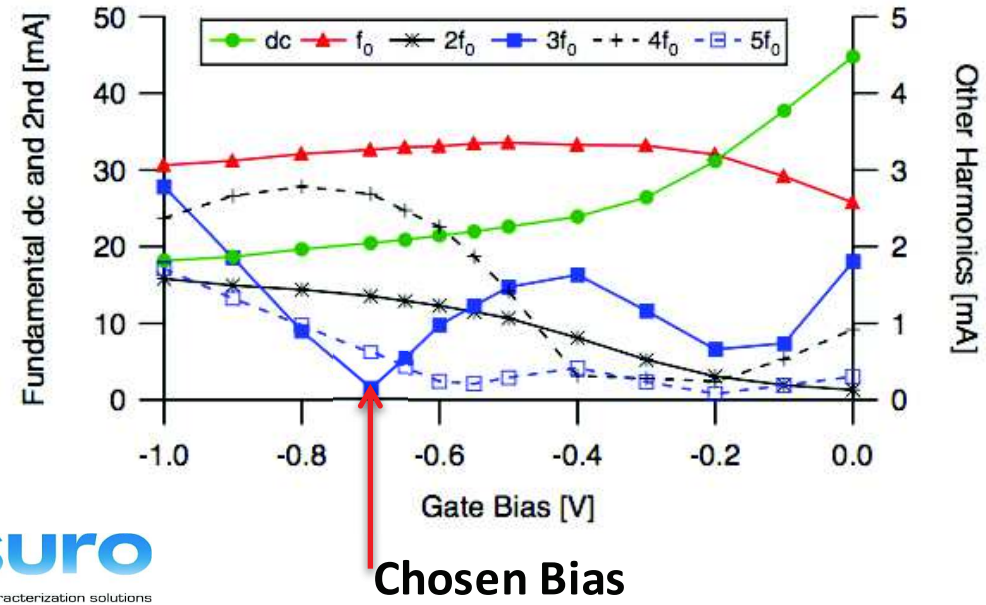
Class	η_{3F0} (%)	10% Knee η	15% Knee η	20% Knee η
B	70.65	63.5	60.05	56.52
F	90	[redacted]	76.5	72

Increasing Knee Voltage

Class F Design Example

- **Step 1 – Engineering the Current Waveform**

- Looking for a Class B current waveform (half rectified with 50% duty cycle).
  - This can be achieved through a combination of gate bias and drive level. Ideally looking for odd harmonic null – Often compromise must be made.

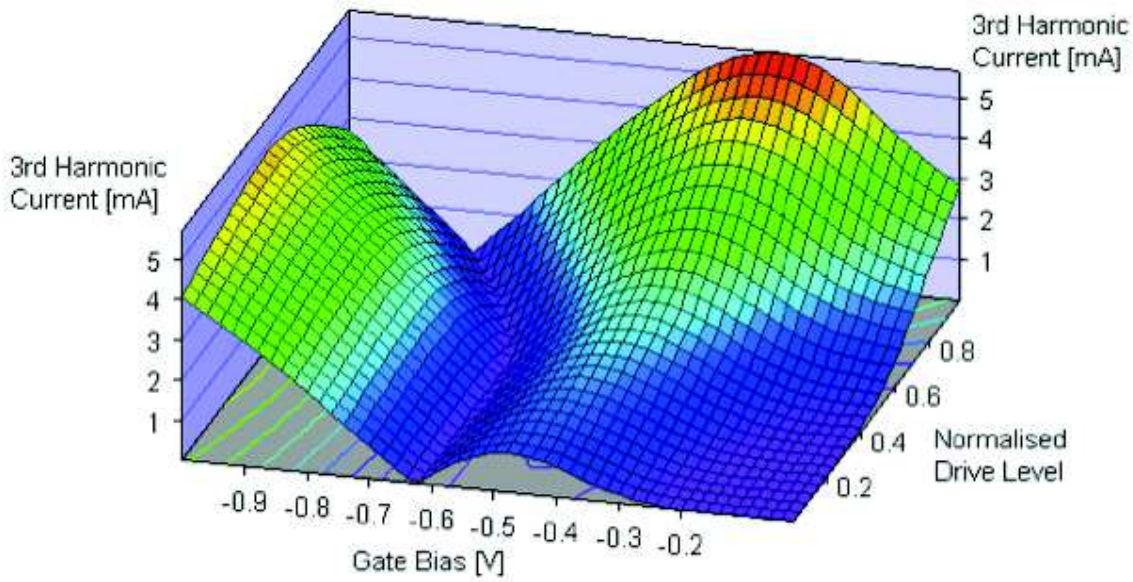


As no ideal case is found 3F0 null is selected – this is essential to obtain the required non-dissipative 3F0 termination.

Class F Design Example

- **Step 1 – Engineering the Current Waveform**

- Note that the harmonic nulls are also a function of drive level, so care must be taken to optimise performance at the desired drive level.



Class F Design Example

- **Step 2 – Engineering the Voltage Waveform (2F0 Termination)**

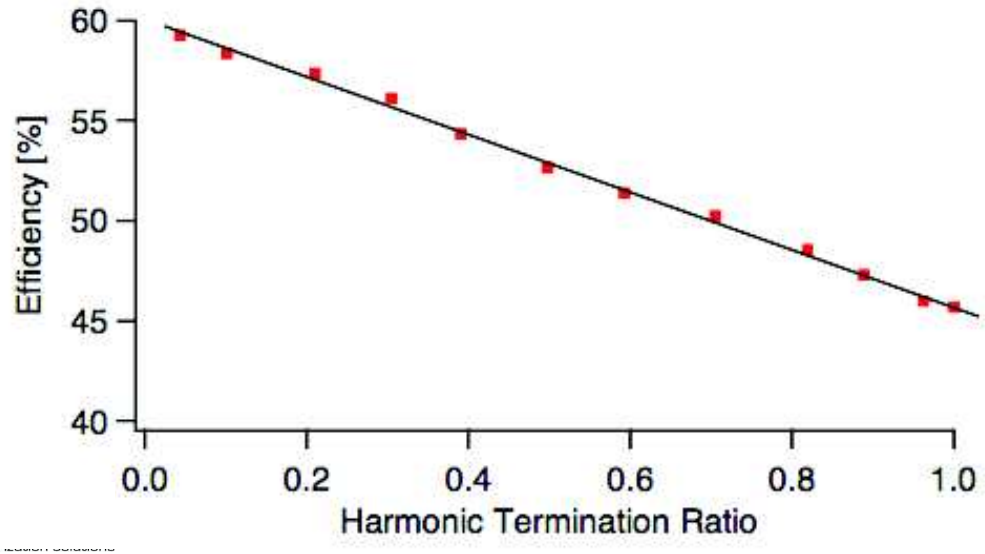
- In a Class F design we are looking for a squared voltage waveform, the next step is properly terminate the second harmonic.

- With device biased to null 3F0, tuning 2nd harmonic to a short circuit, converts the voltage from an inverted half rectified sine wave to a sine wave. Reducing the average DC component, increasing efficiency.

Class F Design Example

- **Step 2 – Engineering the Voltage Waveform (2F0 Termination)**

- Quality of the second harmonic impedance is important, the quality of the open or short circuit termination will depend upon the R_{OPT} of the device.
  - Low Impedance Device, hard to create short circuit
  - High impedance device, hard to create open circuit



Class F Design Example

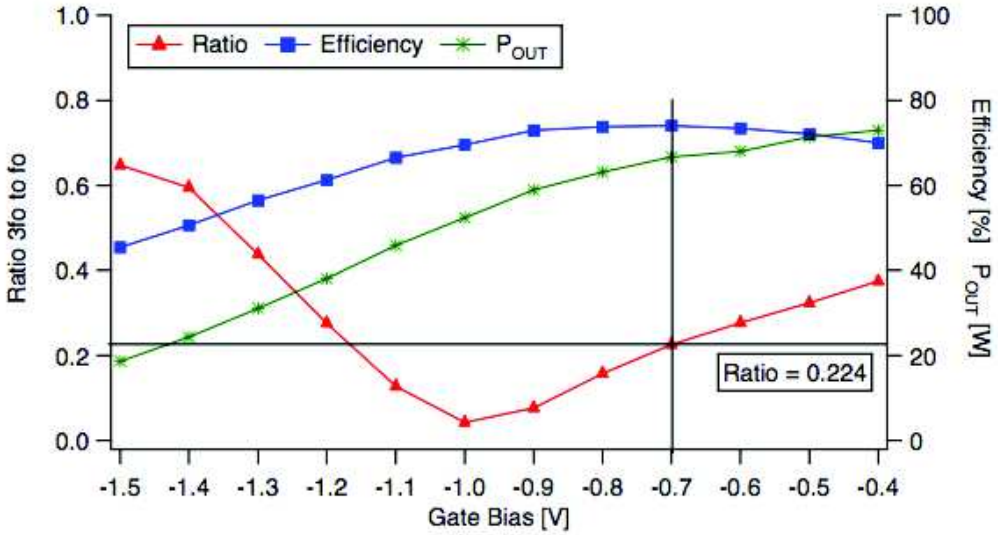
- **Step 3 – Engineering the Voltage Waveform (3F0 Termination/re-optimise F0 Termination)**

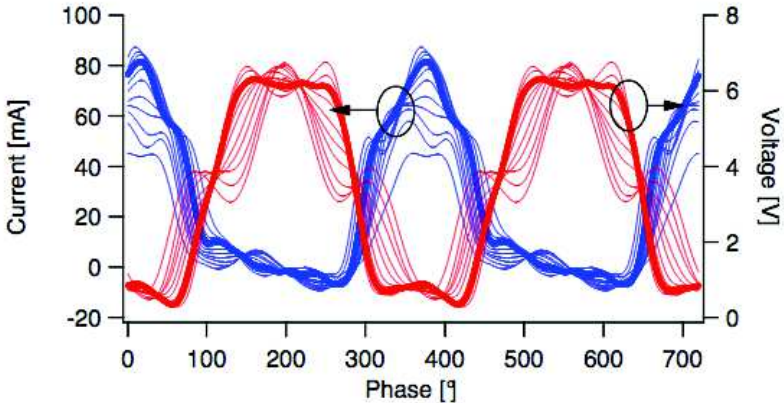
- Final step in the design process is to engineer the third harmonic voltage component, which should be 1/6 the size of the F0 component.
  - Two stages
  - 1. Open circuit at the third harmonic
  - 2. Adjust F0 impedance (R_{OPT} x 4/π) – or equivalent factor for number of harmonics

Class F Design Example

- **Step 3 – Engineering the Voltage Waveform (3F0 Termination/re-optimise F0 Termination)**

- As the third harmonic is an open circuit, not possible to measure third harmonic current, class F can however be confirmed by measuring ratio of 3F0 to F0 voltage (1/6 is optimum)

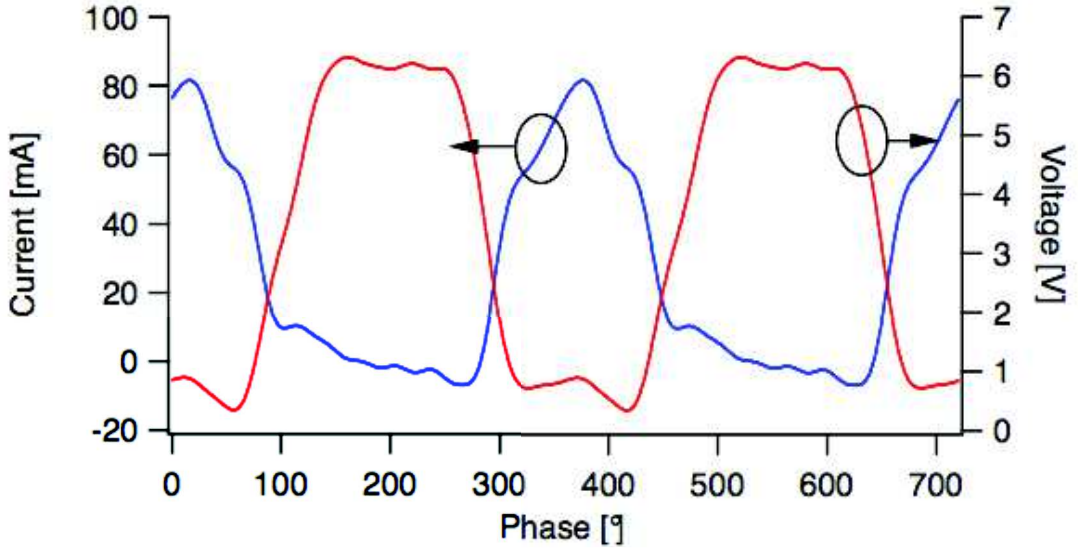


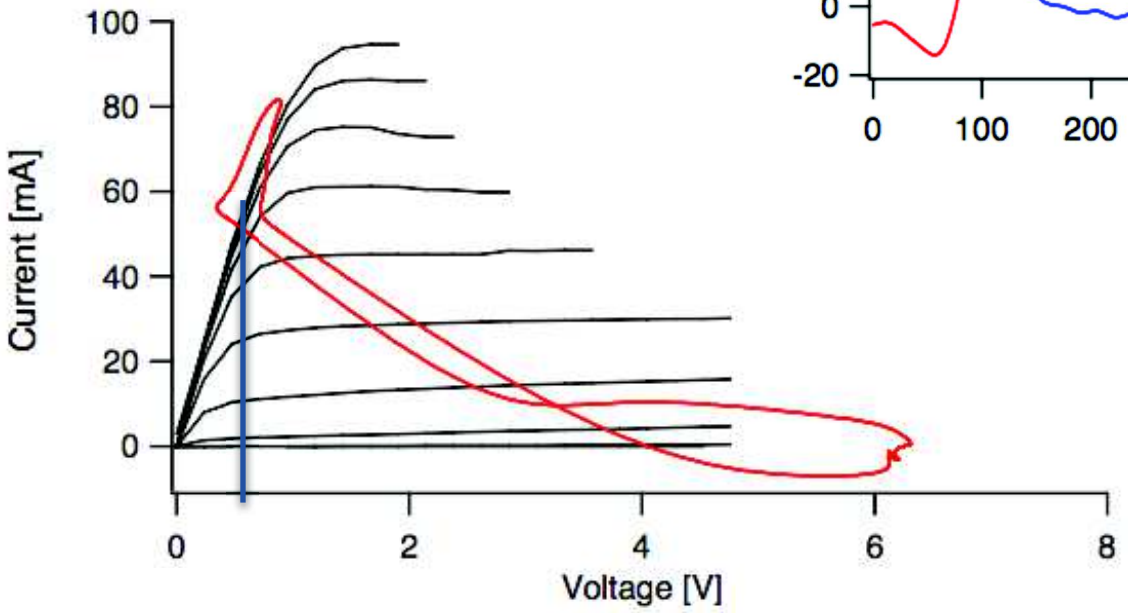


Class F Design Example

- **Results**

Predicted Performance –
$1 – (V_{knee}/ V_{DC}) \times 90.6$
$1 – (0.7/3.5) \times 90.6$
=72.48%





Measured Performance –
Efficiency =75%